LPC1857/53

32-bit ARM Cortex-M3 MCU; up to 1 MB flash and 136 kB SRAM; Ethernet, two High-speed USB, LCD, EMC

Rev. 2 — 15 May 2012 Objective data sheet

1. General description

The LPC1857/53 are ARM Cortex-M3 based microcontrollers for embedded applications. The ARM Cortex-M3 is a next generation core that offers system enhancements such as low power consumption, enhanced debug features, and a high level of support block integration.

The LPC1857/53 operate at CPU frequencies of up to 180 MHz. The ARM Cortex-M3 CPU incorporates a 3-stage pipeline and uses a Harvard architecture with separate local instruction and data buses as well as a third bus for peripherals. The ARM Cortex-M3 CPU also includes an internal prefetch unit that supports speculative branching.

The LPC1857/53 include up to 1 MB of flash and 136 kB of on-chip SRAM, 16 kB of EEPROM memory, a quad SPI Flash Interface (SPIFI), a State Configurable Timer (SCT) subsystem, two High-speed USB controllers, Ethernet, LCD, an external memory controller, and multiple digital and analog peripherals.

2. Features and benefits

- Processor core
  - ARM Cortex-M3 processor, running at CPU frequencies of up to 180 MHz.
  - ARM Cortex-M3 built-in Memory Protection Unit (MPU) supporting eight regions.
  - ARM Cortex-M3 built-in Nested Vectored Interrupt Controller (NVIC).
  - Non-maskable Interrupt (NMI) input.
  - JTAG and Serial Wire Debug, serial trace, eight breakpoints, and four watch points.
  - Enhanced Trace Module (ETM) and Enhanced Trace Buffer (ETB) support.
  - System tick timer.
- On-chip memory
  - Up to 1 MB on-chip dual bank flash memory with flash accelerator.
  - 16 kB on-chip EEPROM data memory.
  - 136 kB SRAM for code and data use.
  - Multiple SRAM blocks with separate bus access.
  - 64 kB ROM containing boot code and on-chip software drivers.
  - 32-bit One-Time Programmable (OTP) memory for general-purpose use.
- Clock generation unit
  - Crystal oscillator with an operating range of 1 MHz to 25 MHz.
  - 12 MHz internal RC oscillator trimmed to 1 % accuracy over temperature and voltage.
  - Ultra-low power RTC crystal oscillator.

    - Three PLLs allow CPU operation up to the maximum CPU rate without the need for a high-frequency crystal. The second PLL is dedicated to the High-speed USB, the third PLL can be used as audio PLL.
    - Clock output.
- Configurable digital peripherals:
    - State Configurable Timer (SCT) subsystem on AHB.
    - Global Input Multiplexer Array (GIMA) allows to cross-connect multiple inputs and outputs to event driven peripherals like timers, SCT, and ADC0/1.
- Serial interfaces:
    - Quad SPI Flash Interface (SPIFI) with 1-, 2-, or 4-bit data at rates of up to 60 MB per second.
    - 10/100T Ethernet MAC with RMII and MII interfaces and DMA support for high throughput at low CPU load. Support for IEEE 1588 time stamping/advanced time stamping (IEEE 1588-2008 v2).
    - One High-speed USB 2.0 Host/Device/OTG interface with DMA support and on-chip high-speed PHY (USB0).
    - One High-speed USB 2.0 Host/Device interface with DMA support, on-chip full-speed PHY and ULPI interface to an external high-speed PHY (USB1).
    - USB interface electrical test software included in ROM USB stack.
    - Four 550 UARTs with DMA support: one UART with full modem interface; one UART with IrDA interface; three USARTs support UART synchronous mode and a smart card interface conforming to ISO7816 specification.
    - Two C_CAN 2.0B controllers with one channel each.
    - Two SSP controllers with FIFO and multi-protocol support. Both SSPs with DMA support.
    - One Fast-mode Plus I^{2}C-bus interface with monitor mode and with open-drain I/O pins conforming to the full I^{2}C-bus specification. Supports data rates of up to 1 Mbit/s.
    - One standard I^{2}C-bus interface with monitor mode and standard I/O pins.
    - Two I^{2}S interfaces with DMA support, each with one input and one output.
- Digital peripherals:
    - External Memory Controller (EMC) supporting external SRAM, ROM, NOR flash, and SDRAM devices.
    - LCD controller with DMA support and a programmable display resolution of up to 1024H × 768V. Supports monochrome and color STN panels and TFT color panels; supports 1/2/4/8 bpp Color Look-Up Table (CLUT) and 16/24-bit direct pixel mapping.
    - SD/MMC card interface.
    - Eight-channel General-Purpose DMA (GPDMA) controller can access all memories on the AHB and all DMA-capable AHB slaves.
    - Up to 164 General-Purpose Input/Output (GPIO) pins with configurable pull-up/pull-down resistors.
    - GPIO registers are located on the AHB for fast access. GPIO ports have DMA support.
    - Up to 8 GPIO pins can be selected from all GPIO pins as edge and level sensitive interrupt sources.

  - Two GPIO group interrupt modules enable an interrupt based on a programmable pattern of input states of a group of GPIO pins.
  - Four general-purpose timer/counters with capture and match capabilities.
  - One motor control PWM for three-phase motor control.
  - One Quadrature Encoder Interface (QEI).
  - Repetitive Interrupt timer (RI timer).
  - Windowed watchdog timer.
  - Ultra-low power Real-Time Clock (RTC) on separate power domain with 256 bytes of battery powered backup registers.
  - Event recorder with three inputs to record event identification and event time; can be battery powered.
  - Alarm timer; can be battery powered.
- Analog peripherals:
  - One 10-bit DAC with DMA support and a data conversion rate of 400 kSamples/s.
  - Two 10-bit ADCs with DMA support and a data conversion rate of 400 kSamples/s. Up to eight input channels per ADC.
- Decryption:
  - Hardware-based AES decryption programmable through an on-chip API.
  - Two 128-bit secure OTP memories for AES key storage and customer use.
  - Random Number Generator (RNG) accessible through AES API.
  - Unique ID for each device.
- Power:
  - Single 3.3 V (2.2 V to 3.6 V) power supply with on-chip internal voltage regulator for the core supply and the RTC power domain.
  - RTC power domain can be powered separately by a 3 V battery supply.
  - Four reduced power modes: Sleep, Deep-sleep, Power-down, and Deep power-down.
  - Processor wake-up from Sleep mode via wake-up interrupts from various peripherals.
  - Wake-up from Deep-sleep, Power-down, and Deep power-down modes via external interrupts and interrupts generated by battery powered blocks in the RTC power domain.
  - Brownout detect with four separate thresholds for interrupt and forced reset.
  - Power-On Reset (POR).
- Available as LQFP208, LBGA256, or TFBGA180 package.

3. Applications

- Industrial
- Consumer
- White goods
- RFID readers
- e-Metering

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
LPC1857FET256	LBGA256	Plastic low profile ball grid array package; 256 balls; body 17 × 17 × 1 mm	SOT740-2
LPC1857FET180	TFBGA180	Thin fine-pitch ball grid array package; 180 balls	SOT570-3
LPC1857FBD208	LQFP208	Plastic low profile quad flat package; 208 leads; body 28 × 28 × 1.4 mm	SOT459-1
LPC1853FET256	LBGA256	Plastic low profile ball grid array package; 256 balls; body 17 × 17 × 1 mm	SOT740-2
LPC1853FET180	TFBGA180	Thin fine-pitch ball grid array package; 180 balls	SOT570-3
LPC1853FBD208	LQFP208	Plastic low profile quad flat package; 208 leads; body 28 × 28 × 1.4 mm	SOT459-1

4.1 Ordering options

Table 2. Ordering options

Type number	Flash	Flash bank A	Flash bank B	Total SRAM	LCD	Ethernet	USB0 (Host, Device, OTG)	USB1 (Host, Device)/ ULPI interface	ADC channels	GPIO
LPC1857FET256	1 MB	512 kB	512 kB	136 kB	yes	yes	yes	yes/yes	8	164
LPC1857FET180	1 MB	512 kB	512 kB	136 kB	yes	yes	yes	yes/yes	8	118
LPC1857FBD208	1 MB	512 kB	512 kB	136 kB	yes	yes	yes	yes/yes	8	142
LPC1853FET256	512 kB	256 kB	256 kB	136 kB	yes	yes	yes	yes/yes	8	164
LPC1853FET180	512 kB	256 kB	256 kB	136 kB	yes	yes	yes	yes/yes	8	118
LPC1853FBD208	512 kB	256 kB	256 kB	136 kB	yes	yes	yes	yes/yes	8	142

5. Block diagram

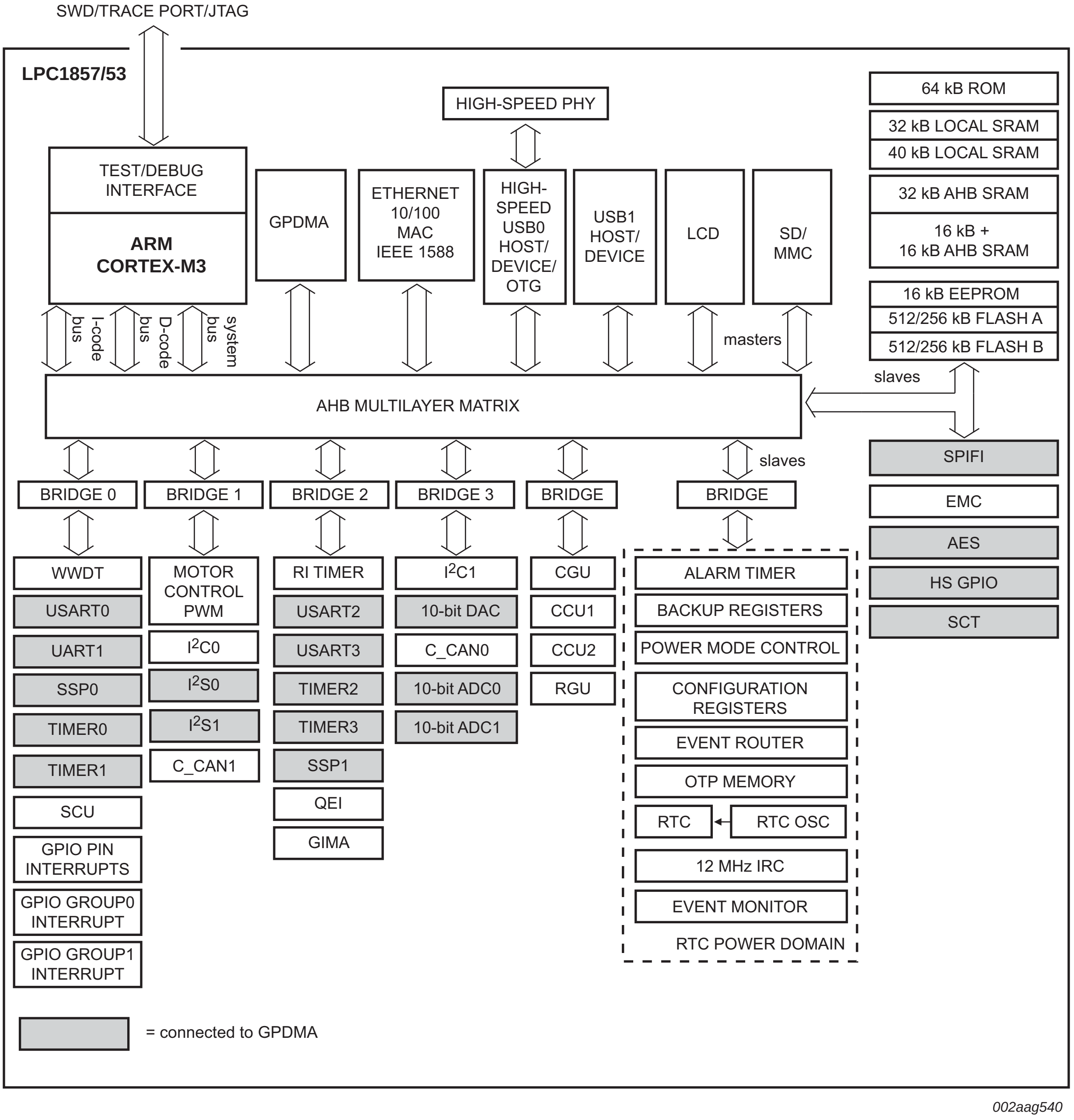


Fig 1. LPC1857/53 block diagram

6. Pinning information

6.1 Pinning

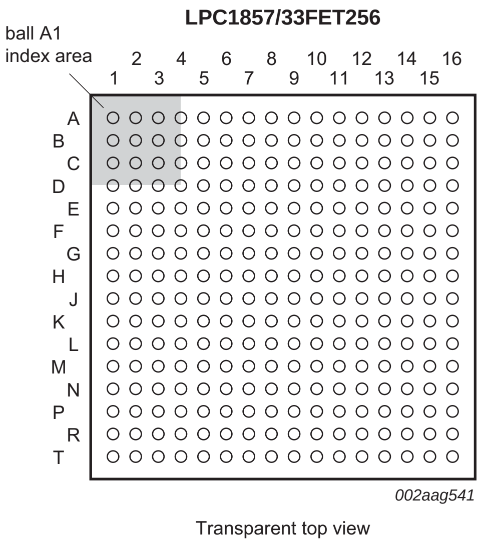


Fig 2. Pin configuration LBGA256 package

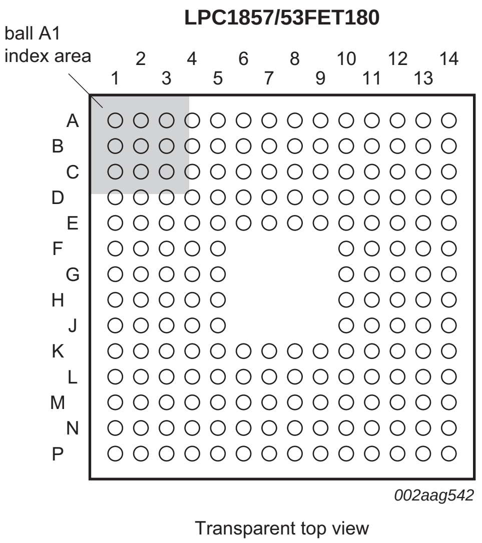


Fig 3. Pin configuration TFBGA180 package

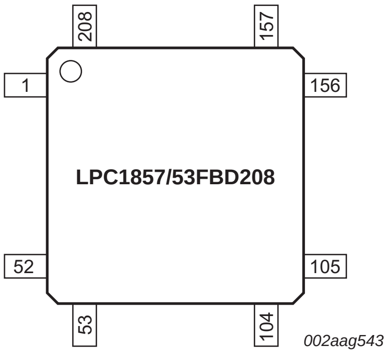


Fig 4. Pin configuration LQFP208 package

6.2 Pin description

On the LPC1857/53, digital pins are grouped into 16 ports, named P0 to P9 and PA to PF, with up to 20 pins used per port. Each digital pin can support up to eight different digital functions, including General Purpose I/O (GPIO), selectable through the SCU registers.

The pin name is not indicative of the GPIO port assigned to it.

Table 3. Pin description

Pin name	LBGA256	TFBGA180	LQFP208		Reset state [1]	Type	Description
Multiplexed digital pins							
P0_0	L3	K3	47	[2]	N; PU	I/O	**GPIO0[0]** — General purpose digital input/output pin.
						I/O	**SSP1_MISO** — Master In Slave Out for SSP1.
						I	**ENET_RXD1** — Ethernet receive data 1 (RMII/MII interface).
						-	**R** — Function reserved.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
						I/O	**I2S0_TX_WS** — Transmit Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I^2S-bus specification*.
						I/O	**I2S1_TX_WS** — Transmit Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I^2S-bus specification*.
P0_1	M2	K2	50	[2]	N; PU	I/O	**GPIO0[1]** — General purpose digital input/output pin.
						I/O	**SSP1_MOSI** — Master Out Slave in for SSP1.
						I	**ENET_COL** — Ethernet Collision detect (MII interface).
						-	**R** — Function reserved.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
							ENET_TX_EN — Ethernet transmit enable (RMII/MII interface).
						I/O	**I2S1_TX_SDA** — I^2S1 transmit data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I^2S-bus specification*.
P1_0	P2	L1	54	[2]	N; PU	I/O	**GPIO0[4]** — General purpose digital input/output pin.
						I	**CTIN_3** — SCT input 3. Capture input 1 of timer 1.
						I/O	**EMC_A5** — External memory address line 5.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
						I/O	**SSP0_SSEL** — Slave Select for SSP0.
						-	**R** — Function reserved.
						I/O	**EMC_D12** — External memory data line 12.
P1_1	R2	N1	58	[2]	N; PU	I/O	**GPIO0[8]** — General purpose digital input/output pin. External boot pin (see Table 5).
						O	**CTOUT_7** — SCT output 7. Match output 3 of timer 1.
						I/O	**EMC_A6** — External memory address line 6.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
						I/O	**SSP0_MISO** — Master In Slave Out for SSP0.
						-	**R** — Function reserved.
						I/O	**EMC_D13** — External memory data line 13.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA180	LQFP208		Reset state [1]	Type	Description
P1_2	R3	N2	60	[2]	N; PU	I/O	**GPIO0[9] —** General purpose digital input/output pin. External boot pin (see Table 5).
						O	**CTOUT_6 —** SCT output 6. Match output 2 of timer 1.
						I/O	**EMC_A7 —** External memory address line 7.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						I/O	**SSP0_MOSI —** Master Out Slave in for SSP0.
						-	**R —** Function reserved.
						I/O	**EMC_D14 —** External memory data line 14.
P1_3	P5	M2	61	[2]	N; PU	I/O	**GPIO0[10] —** General purpose digital input/output pin.
						O	**CTOUT_8 —** SCT output 8. Match output 0 of timer 2.
						-	**R —** Function reserved.
						O	**$\overline{\text{EMC\_OE}}$ —** LOW active Output Enable signal.
						O	**USB0_IND1 —** USB0 port indicator LED control output 1.
						I/O	**SSP1_MISO —** Master In Slave Out for SSP1.
						-	**R —** Function reserved.
						O	**SD_RST —** SD/MMC reset signal for MMC4.4 card.
P1_4	T3	P2	64	[2]	N; PU	I/O	**GPIO0[11] —** General purpose digital input/output pin.
						O	**CTOUT_9 —** SCT output 9. Match output 3 of timer 3.
						-	**R —** Function reserved.
						O	**$\overline{\text{EMC\_BLS0}}$ —** LOW active Byte Lane select signal 0.
						O	**USB0_IND0 —** USB0 port indicator LED control output 0.
						I/O	**SSP1_MOSI —** Master Out Slave in for SSP1.
						I/O	**EMC_D15 —** External memory data line 15.
						O	**SD_VOLT1 —** SD/MMC bus voltage select output 1.
P1_5	R5	N3	65	[2]	N; PU	I/O	**GPIO1[8] —** General purpose digital input/output pin.
						O	**CTOUT_10 —** SCT output 10. Match output 3 of timer 3.
						-	**R —** Function reserved.
						O	**$\overline{\text{EMC\_CS0}}$ —** LOW active Chip Select 0 signal.
						I	**USB0_PWR_FAULT —** Port power fault signal indicating overcurrent condition; this signal monitors over-current on the USB bus (external circuitry required to detect over-current condition).
						I/O	**SSP1_SSEL —** Slave Select for SSP1.
						-	**R —** Function reserved.
						O	**SD_POW —** SD/MMC card power monitor output.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA180	LQFP208		Reset state [1]	Type	Description
P1_6	T4	P3	67	[2]	N; PU	I/O	**GPIO1[9]** — General purpose digital input/output pin.
						I	**CTIN_5** — SCT input 5. Capture input 2 of timer 2.
						-	**R** — Function reserved.
						O	**EMC_WE** — LOW active Write Enable signal.
						-	**R** — Function reserved.
						O	**EMC_BLS0** — LOW active Byte Lane select signal 0.
						-	**R** — Function reserved.
						I/O	**SD_CMD** — SD/MMC command signal.
P1_7	T5	N4	69	[2]	N; PU	I/O	**GPIO1[0]** — General purpose digital input/output pin.
						I	**U1_DSR** — Data Set Ready input for UART1.
						O	**CTOUT_13** — SCT output 13. Match output 3 of timer 3.
						I/O	**EMC_D0** — External memory data line 0.
						O	**USB0_PPWR** — VBUS drive signal (towards external charge pump or power management unit); indicates that VBUS must be driven (active HIGH). Add a pull-down resistor to disable the power switch at reset. This signal has opposite polarity compared to the USB_PPWR used on other NXP LPC parts.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
P1_8	R7	M5	71	[2]	N; PU	I/O	**GPIO1[1]** — General purpose digital input/output pin.
						O	**U1_DTR** — Data Terminal Ready output for UART1.
						O	**CTOUT_12** — SCT output 12. Match output 3 of timer 3.
						I/O	**EMC_D1** — External memory data line 1.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
						O	**SD_VOLT0** — SD/MMC bus voltage select output 0.
P1_9	T7	N5	73	[2]	N; PU	I/O	**GPIO1[2]** — General purpose digital input/output pin.
						O	**U1_RTS** — Request to Send output for UART1.
						O	**CTOUT_11** — SCT output 11. Match output 3 of timer 2.
						I/O	**EMC_D2** — External memory data line 2.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
						I/O	**SD_DAT0** — SD/MMC data bus line 0.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA180	LQFP208		Reset state [1]	Type	Description
P1_10	R8	N6	75	[2]	N; PU	I/O	**GPIO1[3]** — General purpose digital input/output pin.
						I	**U1_RI** — Ring Indicator input for UART1.
						O	**CTOUT_14** — SCT output 14. Match output 2 of timer 3.
						I/O	**EMC_D3** — External memory data line 3.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
						I/O	**SD_DAT1** — SD/MMC data bus line 1.
P1_11	T9	P8	77	[2]	N; PU	I/O	**GPIO1[4]** — General purpose digital input/output pin.
						I	**U1_CTS** — Clear to Send input for UART1.
						O	**CTOUT_15** — SCT output 15. Match output 3 of timer 3.
						I/O	**EMC_D4** — External memory data line 4.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
						I/O	**SD_DAT2** — SD/MMC data bus line 2.
P1_12	R9	P7	78	[2]	N; PU	I/O	**GPIO1[5]** — General purpose digital input/output pin.
						I	**U1_DCD** — Data Carrier Detect input for UART1.
						-	**R** — Function reserved.
						I/O	**EMC_D5** — External memory data line 5.
						I	**T0_CAP1** — Capture input 1 of timer 0.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
						I/O	**SD_DAT3** — SD/MMC data bus line 3.
P1_13	R10	D6	83	[2]	N; PU	I/O	**GPIO1[6]** — General purpose digital input/output pin.
						O	**U1_TXD** — Transmitter output for UART1.
						-	**R** — Function reserved.
						I/O	**EMC_D6** — External memory data line 6.
						I	**T0_CAP0** — Capture input 0 of timer 0.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
						I	**SD_CD** — SD/MMC card detect input.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA180	LQFP208		Reset state [1]	Type	Description
P1_14	R11	K7	85	[2]	N; PU	I/O	**GPIO1[7]** — General purpose digital input/output pin.
						I	**U1_RXD** — Receiver input for UART1.
						-	**R** — Function reserved.
						I/O	**EMC_D7** — External memory data line 7.
						O	**T0_MAT2** — Match output 2 of timer 0.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
P1_15	T12	P11	87	[2]	N; PU	I/O	**GPIO0[2]** — General purpose digital input/output pin.
						O	**U2_TXD** — Transmitter output for USART2.
						-	**R** — Function reserved.
						I	**ENET_RXD0** — Ethernet receive data 0 (RMII/MII interface).
						O	**T0_MAT1** — Match output 1 of timer 0.
						-	**R** — Function reserved.
						I/O	**EMC_D8** — External memory data line 8.
						-	**R** — Function reserved.
P1_16	M7	L5	90	[2]	N; PU	I/O	**GPIO0[3]** — General purpose digital input/output pin.
						I	**U2_RXD** — Receiver input for USART2.
						-	**R** — Function reserved.
						I	**ENET_CRS** — Ethernet Carrier Sense (MII interface).
						O	**T0_MAT0** — Match output 0 of timer 0.
						-	**R** — Function reserved.
						I/O	**EMC_D9** — External memory data line 9.
						I	**ENET_RX_DV** — Ethernet Receive Data Valid (RMII/MII interface).
P1_17	M8	L6	93	[3]	N; PU	I/O	**GPIO0[12]** — General purpose digital input/output pin.
						I/O	**U2_UCLK** — Serial clock input/output for USART2 in synchronous mode.
						-	**R** — Function reserved.
						I/O	**ENET_MDIO** — Ethernet MIIM data input and output.
						I	**T0_CAP3** — Capture input 3 of timer 0.
						O	**CAN1_TD** — CAN1 transmitter output.
						-	**R** — Function reserved.
						-	**R** — Function reserved.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA180	LQFP208		Reset state [1]	Type	Description
P1_18	N12	N10	95	[2]	N; PU	I/O	**GPIO0[13]** — General purpose digital input/output pin.
						I/O	**U2_DIR** — RS-485/EIA-485 output enable/direction control for USART2.
						-	**R** — Function reserved.
						O	**ENET_TXD0** — Ethernet transmit data 0 (RMII/MII interface).
						O	**T0_MAT3** — Match output 3 of timer 0.
						I	**CAN1_RD** — CAN1 receiver input.
						-	**R** — Function reserved.
						I/O	**EMC_D10** — External memory data line 10.
P1_19	M11	N9	96	[2]	N; PU	I	**ENET_TX_CLK (ENET_REF_CLK)** — Ethernet Transmit Clock (MII interface) or Ethernet Reference Clock (RMII interface).
						I/O	**SSP1_SCK** — Serial clock for SSP1.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
						O	**CLKOUT** — Clock output pin.
						-	**R** — Function reserved.
						O	**I2S0_RX_MCLK** — I^{2}S receive master clock.
						I/O	**I2S1_TX_SCK** — Transmit Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the *I^{2}S-bus specification*.
P1_20	M10	J10	100	[2]	N; PU	I/O	**GPIO0[15]** — General purpose digital input/output pin.
						I/O	**SSP1_SSEL** — Slave Select for SSP1.
						-	**R** — Function reserved.
						O	**ENET_TXD1** — Ethernet transmit data 1 (RMII/MII interface).
						I	**T0_CAP2** — Capture input 2 of timer 0.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
						I/O	**EMC_D11** — External memory data line 11.
P2_0	T16	N14	108	[2]	N; PU	-	**R** — Function reserved.
						O	**U0_TXD** — Transmitter output for USART0. See Table 4 for ISP mode.
						I/O	**EMC_A13** — External memory address line 13.
						O	**USB0_PPWR** — VBUS drive signal (towards external charge pump or power management unit); indicates that VBUS must be driven (active HIGH). Add a pull-down resistor to disable the power switch at reset. This signal has opposite polarity compared to the $\overline{\text{USB\_PPWR}}$ used on other NXP LPC parts.
						I/O	**GPIO5[0]** — General purpose digital input/output pin.
						-	**R** — Function reserved.
						I	**T3_CAP0** — Capture input 0 of timer 3.
						O	**ENET_MDC** — Ethernet MIIM clock.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA180	LQFP208		Reset state [1]	Type	Description
P2_1	N15	M13	116	[2]	N; PU	-	**R** — Function reserved.
						I	**U0_RXD** — Receiver input for USART0. See Table 4 for ISP mode.
						I/O	**EMC_A12** — External memory address line 12.
						I	**USB0_PWR_FAULT** — Port power fault signal indicating overcurrent condition; this signal monitors over-current on the USB bus (external circuitry required to detect over-current condition).
						I/O	**GPIO5[1]** — General purpose digital input/output pin.
						-	**R** — Function reserved.
						I	**T3_CAP1** — Capture input 1 of timer 3.
						-	**R** — Function reserved.
P2_2	M15	L13	121	[2]	N; PU	-	**R** — Function reserved.
						I/O	**U0_UCLK** — Serial clock input/output for USART0 in synchronous mode.
						I/O	**EMC_A11** — External memory address line 11.
						O	**USB0_IND1** — USB0 port indicator LED control output 1.
						I/O	**GPIO5[2]** — General purpose digital input/output pin.
						I	**CTIN_6** — SCT input 6. Capture input 1 of timer 3.
						I	**T3_CAP2** — Capture input 2 of timer 3.
						O	**EMC_CS1** — LOW active Chip Select 1 signal.
P2_3	J12	G11	127	[3]	N; PU	-	**R** — Function reserved.
						I/O	**I2C1_SDA** — I^{2}C1 data input/output (this pin does not use a specialized I^{2}C pad).
						O	**U3_TXD** — Transmitter output for USART3. See Table 4 for ISP mode.
						I	**CTIN_1** — SCT input 1. Capture input 1 of timer 0. Capture input 1 of timer 2.
						I/O	**GPIO5[3]** — General purpose digital input/output pin.
						-	**R** — Function reserved.
						O	**T3_MAT0** — Match output 0 of timer 3.
						O	**USB0_PPWR** — VBUS drive signal (towards external charge pump or power management unit); indicates that VBUS must be driven (active HIGH). Add a pull-down resistor to disable the power switch at reset. This signal has opposite polarity compared to the USB_PPWR used on other NXP LPC parts.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA180	LQFP208		Reset state [1]	Type	Description
P2_4	K11	L9	128	[3]	N; PU	-	**R —** Function reserved.
						I/O	**I2C1_SCL —** I^{2}C1 clock input/output (this pin does not use a specialized I^{2}C pad).
						I	**U3_RXD —** Receiver input for USART3. See Table 4 for ISP mode.
						I	**CTIN_0 —** SCT input 0. Capture input 0 of timer 0, 1, 2, 3.
						I/O	**GPIO5[4] —** General purpose digital input/output pin.
						-	**R —** Function reserved.
						O	**T3_MAT1 —** Match output 1 of timer 3.
						I	**USB0_PWR_FAULT —** Port power fault signal indicating overcurrent condition; this signal monitors over-current on the USB bus (external circuitry required to detect over-current condition).
P2_5	K14	J12	131	[3]	N; PU	-	**R —** Function reserved.
						I	**CTIN_2 —** SCT input 2. Capture input 2 of timer 0.
						I	**USB1_VBUS —** Monitors the presence of USB1 bus power. **Note:** This signal must be HIGH for USB reset to occur.
						I	**ADCTRIG1 —** ADC trigger input 1.
						I/O	**GPIO5[5] —** General purpose digital input/output pin.
						-	**R —** Function reserved.
						O	**T3_MAT2 —** Match output 2 of timer 3.
						O	**USB0_IND0 —** USB0 port indicator LED control output 0.
P2_6	K16	J14	137	[2]	N; PU	-	**R —** Function reserved.
						I/O	**U0_DIR —** RS-485/EIA-485 output enable/direction control for USART0.
						I/O	**EMC_A10 —** External memory address line 10.
						O	**USB0_IND0 —** USB0 port indicator LED control output 0.
						I/O	**GPIO5[6] —** General purpose digital input/output pin.
						I	**CTIN_7 —** SCT input 7.
						I	**T3_CAP3 —** Capture input 3 of timer 3.
						O	**EMC_BLS1 —** LOW active Byte Lane select signal 1.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA180	LQFP208		Reset state [1]	Type	Description
P2_7	H14	G12	138	[2]	N; PU	I/O	**GPIO0[7]** — General purpose digital input/output pin. ISP entry pin. If this pin is pulled LOW at reset, the part enters ISP mode or boots from an external source (see Table 4 and Table 5).
						O	**CTOUT_1** — SCT output 1. Match output 3 of timer 3.
						I/O	**U3_UCLK** — Serial clock input/output for USART3 in synchronous mode.
						I/O	**EMC_A9** — External memory address line 9.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
						O	**T3_MAT3** — Match output 3 of timer 3.
						-	**R** — Function reserved.
P2_8	J16	H14	140	[2]	N; PU	-	**R** — Function reserved. External boot pin (see Table 5)
						O	**CTOUT_0** — SCT output 0. Match output 0 of timer 0.
						I/O	**U3_DIR** — RS-485/EIA-485 output enable/direction control for USART3.
						I/O	**EMC_A8** — External memory address line 8.
						I/O	**GPIO5[7]** — General purpose digital input/output pin.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
P2_9	H16	G14	144	[2]	N; PU	I/O	**GPIO1[10]** — General purpose digital input/output pin. External boot pin (see Table 5).
						O	**CTOUT_3** — SCT output 3. Match output 3 of timer 0.
						I/O	**U3_BAUD** — Baud pin for USART3.
						I/O	**EMC_A0** — External memory address line 0.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
P2_10	G16	F14	146	[2]	N; PU	I/O	**GPIO0[14]** — General purpose digital input/output pin.
						O	**CTOUT_2** — SCT output 2. Match output 2 of timer 0.
						O	**U2_TXD** — Transmitter output for USART2.
						I/O	**EMC_A1** — External memory address line 1.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
						-	**R** — Function reserved.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA180	LQFP208		Reset state [1]	Type	Description
P2_11	F16	E13	148	[2]	N; PU	I/O	**GPIO1[11] —** General purpose digital input/output pin.
						O	**CTOUT_5 —** SCT output 5. Match output 3 of timer 3.
						I	**U2_RXD —** Receiver input for USART2.
						I/O	**EMC_A2 —** External memory address line 2.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
P2_12	E15	D13	153	[2]	N; PU	I/O	**GPIO1[12] —** General purpose digital input/output pin.
						O	**CTOUT_4 —** SCT output 4. Match output 3 of timer 3.
						-	**R —** Function reserved.
						I/O	**EMC_A3 —** External memory address line 3.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						I/O	**U2_UCLK —** Serial clock input/output for USART2 in synchronous mode.
P2_13	C16	E14	156	[2]	N; PU	I/O	**GPIO1[13] —** General purpose digital input/output pin.
						I	**CTIN_4 —** SCT input 4. Capture input 2 of timer 1.
						-	**R —** Function reserved.
						I/O	**EMC_A4 —** External memory address line 4.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						I/O	**U2_DIR —** RS-485/EIA-485 output enable/direction control for USART2.
P3_0	F13	D12	161	[2]	N; PU	I/O	**I2S0_RX_SCK —** I^{2}S receive clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the *I^{2}S-bus specification*.
						O	**I2S0_RX_MCLK —** I^{2}S receive master clock.
						I/O	**I2S0_TX_SCK —** Transmit Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the *I^{2}S-bus specification*.
						O	**I2S0_TX_MCLK —** I^{2}S transmit master clock.
						I/O	**SSP0_SCK —** Serial clock for SSP0.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						-	**R —** Function reserved.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA180	LQFP208		Reset state [1]	Type	Description
P3_1	G11	D10	163	[2]	N; PU	I/O	**I2S0_TX_WS —** Transmit Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I^2S-bus specification*.
						I/O	**I2S0_RX_WS —** Receive Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I^2S-bus specification*.
						I	**CAN0_RD —** CAN receiver input.
						O	**USB1_IND1 —** USB1 Port indicator LED control output 1.
						I/O	**GPIO5[8] —** General purpose digital input/output pin.
						-	**R —** Function reserved.
						O	**LCD_VD15 —** LCD data.
						-	**R —** Function reserved.
P3_2	F11	D9	166	[2]	OL; PU	I/O	**I2S0_TX_SDA —** I^2S transmit data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I^2S-bus specification*.
						I/O	**I2S0_RX_SDA —** I^2S Receive data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I^2S-bus specification*.
						O	**CAN0_TD —** CAN transmitter output.
						O	**USB1_IND0 —** USB1 Port indicator LED control output 0.
						I/O	**GPIO5[9] —** General purpose digital input/output pin.
						-	**R —** Function reserved.
						O	**LCD_VD14 —** LCD data.
						-	**R —** Function reserved.
P3_3	B14	B13	169	[4]	N; PU	-	**R —** Function reserved.
						-	**R —** Function reserved.
						I/O	**SSP0_SCK —** Serial clock for SSP0.
						O	**SPIFI_SCK —** Serial clock for SPIFI.
						O	**CGU_OUT1 —** CGU spare clock output 1.
						-	**R —** Function reserved.
						O	**I2S0_TX_MCLK —** I^2S transmit master clock.
						I/O	**I2S1_TX_SCK —** Transmit Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the *I^2S-bus specification*.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA180	LQFP208		Reset state [1]	Type	Description
P3_4	A15	C14	171	[2]	N; PU	I/O	**GPIO1[14]** — General purpose digital input/output pin.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
						I/O	**SPIFI_SIO3** — I/O lane 3 for SPIFI.
						O	**U1_TXD** — Transmitter output for UART1.
						I/O	**I2S0_TX_WS** — Transmit Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I^{2}S-bus specification*.
						I/O	**I2S1_RX_SDA** — I^{2}S1 Receive data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I^{2}S-bus specification*.
						O	**LCD_VD13** — LCD data.
P3_5	C12	C11	173	[2]	N; PU	I/O	**GPIO1[15]** — General purpose digital input/output pin.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
						I/O	**SPIFI_SIO2** — I/O lane 2 for SPIFI.
						I	**U1_RXD** — Receiver input for UART1.
						I/O	**I2S0_TX_SDA** — I^{2}S transmit data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I^{2}S-bus specification*.
						I/O	**I2S1_RX_WS** — Receive Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I^{2}S-bus specification*.
						O	**LCD_VD12** — LCD data.
P3_6	B13	B12	174	[2]	N; PU	I/O	**GPIO0[6]** — General purpose digital input/output pin.
						-	**R** — Function reserved.
						I/O	**SSP0_SSEL** — Slave Select for SSP0.
						I/O	**SPIFI_MISO** — Input 1 in SPIFI quad mode; SPIFI output IO1.
						-	**R** — Function reserved.
						I/O	**SSP0_MISO** — Master In Slave Out for SSP0.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
P3_7	C11	C10	176	[2]	N; PU	-	**R** — Function reserved.
						-	**R** — Function reserved.
						I/O	**SSP0_MISO** — Master In Slave Out for SSP0.
						I/O	**SPIFI_MOSI** — Input 0 in SPIFI quad mode; SPIFI output IO0.
						I/O	**GPIO5[10]** — General purpose digital input/output pin.
						I/O	**SSP0_MOSI** — Master Out Slave in for SSP0.
						-	**R** — Function reserved.
						-	**R** — Function reserved.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA180	LQFP208		Reset state [1]	Type	Description
P3_8	C10	C9	179	[2]	N; PU	-	**R** — Function reserved.
						-	**R** — Function reserved.
						I/O	**SSP0_MOSI** — Master Out Slave in for SSP0.
						I/O	**SPIFI_CS** — SPIFI serial flash chip select.
						I/O	**GPIO5[11]** — General purpose digital input/output pin.
						I/O	**SSP0_SSEL** — Slave Select for SSP0.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
P4_0	D5	D4	1	[2]	N; PU	I/O	**GPIO2[0]** — General purpose digital input/output pin.
						O	**MCOA0** — Motor control PWM channel 0, output A.
						I	**NMI** — External interrupt input to NMI.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
						O	**LCD_VD13** — LCD data.
						I/O	**U3_UCLK** — Serial clock input/output for USART3 in synchronous mode.
						-	**R** — Function reserved.
P4_1	A1	D3	3	[5]	N; PU	I/O	**GPIO2[1]** — General purpose digital input/output pin.
						O	**CTOUT_1** — SCT output 1. Match output 3 of timer 3.
						O	**LCD_VD0** — LCD data.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
						O	**LCD_VD19** — LCD data.
						O	**U3_TXD** — Transmitter output for USART3.
						I	**ENET_COL** — Ethernet Collision detect (MII interface).
						AI	**ADC0_1** — ADC0, input channel 1. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC.
P4_2	D3	A2	12	[2]	N; PU	I/O	**GPIO2[2]** — General purpose digital input/output pin.
						O	**CTOUT_0** — SCT output 0. Match output 0 of timer 0.
						O	**LCD_VD3** — LCD data.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
						O	**LCD_VD12** — LCD data.
						I	**U3_RXD** — Receiver input for USART3.
						-	**R** — Function reserved.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA180	LQFP208		Reset state [1]	Type	Description
P4_3	C2	B2	10	[5]	N; PU	I/O	**GPIO2[3]** — General purpose digital input/output pin.
						O	**CTOUT_3** — SCT output 3. Match output 3 of timer 0.
						O	**LCD_VD2** — LCD data.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
						O	**LCD_VD21** — LCD data.
						I/O	**U3_BAUD** — Baud pin for USART3.
						-	**R** — Function reserved.
						AI	**ADC0_0** — ADC0, input channel 0. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC.
P4_4	B1	A1	14	[5]	N; PU	I/O	**GPIO2[4]** — General purpose digital input/output pin.
						O	**CTOUT_2** — SCT output 2. Match output 2 of timer 0.
						O	**LCD_VD1** — LCD data.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
						O	**LCD_VD20** — LCD data.
						I/O	**U3_DIR** — RS-485/EIA-485 output enable/direction control for USART3.
						-	**R** — Function reserved.
						AO	**DAC** — DAC output. Configure the pin as GPIO input and use the analog function select register in the SCU to select the DAC.
P4_5	D2	C2	15	[2]	N; PU	I/O	**GPIO2[5]** — General purpose digital input/output pin.
						O	**CTOUT_5** — SCT output 5. Match output 3 of timer 3.
						O	**LCD_FP** — Frame pulse (STN). Vertical synchronization pulse (TFT).
						-	**R** — Function reserved.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
P4_6	C1	B1	17	[2]	N; PU	I/O	**GPIO2[6]** — General purpose digital input/output pin.
						O	**CTOUT_4** — SCT output 4. Match output 3 of timer 3.
						O	**LCD_ENAB/LCDM** — STN AC bias drive or TFT data enable input.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
						-	**R** — Function reserved.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA180	LQFP208		Reset state [1]	Type	Description
P4_7	H4	F4	21	[2]	O; PU	O	**LCD_DCLK** — LCD panel clock.
						I	**GP_CLKIN** — General purpose clock input to the CGU.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
						I/O	**I2S1_TX_SCK** — Transmit Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the *I²S-bus specification*.
						I/O	**I2S0_TX_SCK** — Transmit Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the *I²S-bus specification*.
P4_8	E2	D2	23	[2]	N; PU	-	**R** — Function reserved.
						I	**CTIN_5** — SCT input 5. Capture input 2 of timer 2.
						O	**LCD_VD9** — LCD data.
						-	**R** — Function reserved.
						I/O	**GPIO5[12]** — General purpose digital input/output pin.
						O	**LCD_VD22** — LCD data.
						O	**CAN1_TD** — CAN1 transmitter output.
						-	**R** — Function reserved.
P4_9	L2	J2	48	[2]	N; PU	-	**R** — Function reserved.
						I	**CTIN_6** — SCT input 6. Capture input 1 of timer 3.
						O	**LCD_VD11** — LCD data.
						-	**R** — Function reserved.
						I/O	**GPIO5[13]** — General purpose digital input/output pin.
						O	**LCD_VD15** — LCD data.
						I	**CAN1_RD** — CAN1 receiver input.
						-	**R** — Function reserved.
P4_10	M3	L3	51	[2]	N; PU	-	**R** — Function reserved.
						I	**CTIN_2** — SCT input 2. Capture input 2 of timer 0.
						O	**LCD_VD10** — LCD data.
						-	**R** — Function reserved.
						I/O	**GPIO5[14]** — General purpose digital input/output pin.
						O	**LCD_VD14** — LCD data.
						-	**R** — Function reserved.
						-	**R** — Function reserved.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA180	LQFP208		Reset state [1]	Type	Description
P5_0	N3	L2	53	[2]	N; PU	I/O	**GPIO2[9]** — General purpose digital input/output pin.
						O	**MCOB2** — Motor control PWM channel 2, output B.
						I/O	**EMC_D12** — External memory data line 12.
						-	**R** — Function reserved.
						I	**U1_DSR** — Data Set Ready input for UART1.
						I	**T1_CAP0** — Capture input 0 of timer 1.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
P5_1	P3	M1	55	[2]	N; PU	I/O	**GPIO2[10]** — General purpose digital input/output pin.
						I	**MCI2** — Motor control PWM channel 2, input.
						I/O	**EMC_D13** — External memory data line 13.
						-	**R** — Function reserved.
						O	**U1_DTR** — Data Terminal Ready output for UART1. Can also be configured to be an RS-485/EIA-485 output enable signal for UART1.
						I	**T1_CAP1** — Capture input 1 of timer 1.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
P5_2	R4	M3	63	[2]	N; PU	I/O	**GPIO2[11]** — General purpose digital input/output pin.
						I	**MCI1** — Motor control PWM channel 1, input.
						I/O	**EMC_D14** — External memory data line 14.
						-	**R** — Function reserved.
						O	**U1_RTS** — Request to Send output for UART1. Can also be configured to be an RS-485/EIA-485 output enable signal for UART1.
						I	**T1_CAP2** — Capture input 2 of timer 1.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
P5_3	T8	P6	76	[2]	N; PU	I/O	**GPIO2[12]** — General purpose digital input/output pin.
						I	**MCI0** — Motor control PWM channel 0, input.
						I/O	**EMC_D15** — External memory data line 15.
						-	**R** — Function reserved.
						I	**U1_RI** — Ring Indicator input for UART1.
						I	**T1_CAP3** — Capture input 3 of timer 1.
						-	**R** — Function reserved.
						-	**R** — Function reserved.

Table 3. Pin description ...*continued*

Pin name	LBGA256	TFBGA180	LQFP208		Reset state [1]	Type	Description
P5_4	P9	N7	80	[2]	N; PU	I/O	**GPIO2[13] —** General purpose digital input/output pin.
						O	**MCOB0 —** Motor control PWM channel 0, output B.
						I/O	**EMC_D8 —** External memory data line 8.
						-	**R —** Function reserved.
						I	**U1_CTS —** Clear to Send input for UART1.
						O	**T1_MAT0 —** Match output 0 of timer 1.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
P5_5	P10	N8	81	[2]	N; PU	I/O	**GPIO2[14] —** General purpose digital input/output pin.
						O	**MCOA1 —** Motor control PWM channel 1, output A.
						I/O	**EMC_D9 —** External memory data line 9.
						-	**R —** Function reserved.
						I	**U1_DCD —** Data Carrier Detect input for UART1.
						O	**T1_MAT1 —** Match output 1 of timer 1.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
P5_6	T13	M11	89	[2]	N; PU	I/O	**GPIO2[15] —** General purpose digital input/output pin.
						O	**MCOB1 —** Motor control PWM channel 1, output B.
						I/O	**EMC_D10 —** External memory data line 10.
						-	**R —** Function reserved.
						O	**U1_TXD —** Transmitter output for UART1.
						O	**T1_MAT2 —** Match output 2 of timer 1.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
P5_7	R12	N11	91	[2]	N; PU	I/O	**GPIO2[7] —** General purpose digital input/output pin.
						O	**MCOA2 —** Motor control PWM channel 2, output A.
						I/O	**EMC_D11 —** External memory data line 11.
						-	**R —** Function reserved.
						I	**U1_RXD —** Receiver input for UART1.
						O	**T1_MAT3 —** Match output 3 of timer 1.
						-	**R —** Function reserved.
						-	**R —** Function reserved.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA180	LQFP208		Reset state [1]	Type	Description
P6_0	M12	M10	105	[2]	N; PU	-	**R —** Function reserved.
						O	**I2S0_RX_MCLK —** I^{2}S receive master clock.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						I/O	**I2S0_RX_SCK —** Receive Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the *I^{2}S-bus specification*.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
P6_1	R15	P14	107	[2]	N; PU	I/O	**GPIO3[0] —** General purpose digital input/output pin.
						O	**EMC_DYCS1 —** SDRAM chip select 1.
						I/O	**U0_UCLK —** Serial clock input/output for USART0 in synchronous mode.
						I/O	**I2S0_RX_WS —** Receive Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I^{2}S-bus specification*.
						-	**R —** Function reserved.
						I	**T2_CAP0 —** Capture input 2 of timer 2.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
P6_2	L13	K11	111	[2]	N; PU	I/O	**GPIO3[1] —** General purpose digital input/output pin.
						O	**EMC_CKEOUT1 —** SDRAM clock enable 1.
						I/O	**U0_DIR —** RS-485/EIA-485 output enable/direction control for USART0.
						I/O	**I2S0_RX_SDA —** I^{2}S Receive data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I^{2}S-bus specification*.
						-	**R —** Function reserved.
						I	**T2_CAP1 —** Capture input 1 of timer 2.
						-	**R —** Function reserved.
						-	**R —** Function reserved.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA180	LQFP208		Reset state [1]	Type	Description
P6_3	P15	N13	113	[2]	N; PU	I/O	**GPIO3[2]** — General purpose digital input/output pin.
						O	**USB0_PPWR** — VBUS drive signal (towards external charge pump or power management unit); indicates that VBUS must be driven (active HIGH). Add a pull-down resistor to disable the power switch at reset. This signal has opposite polarity compared to the $\overline{\text{USB\_PPWR}}$ used on other NXP LPC parts.
						-	**R** — Function reserved.
						O	**$\overline{\text{EMC\_CS1}}$** — LOW active Chip Select 1 signal.
						-	**R** — Function reserved.
						I	**T2_CAP2** — Capture input 2 of timer 2.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
P6_4	R16	M14	114	[2]	N; PU	I/O	**GPIO3[3]** — General purpose digital input/output pin.
						I	**CTIN_6** — SCT input 6. Capture input 1 of timer 3.
						O	**U0_TXD** — Transmitter output for USART0.
						O	**$\overline{\text{EMC\_CAS}}$** — LOW active SDRAM Column Address Strobe.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
P6_5	P16	L14	117	[2]	N; PU	I/O	**GPIO3[4]** — General purpose digital input/output pin.
						O	**CTOUT_6** — SCT output 6. Match output 2 of timer 1.
						I	**U0_RXD** — Receiver input for USART0.
						O	**$\overline{\text{EMC\_RAS}}$** — LOW active SDRAM Row Address Strobe.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
P6_6	L14	K12	119	[2]	N; PU	I/O	**GPIO0[5]** — General purpose digital input/output pin.
						O	**$\overline{\text{EMC\_BLS1}}$** — LOW active Byte Lane select signal 1.
						-	**R** — Function reserved.
						I	**USB0_PWR_FAULT** — Port power fault signal indicating overcurrent condition; this signal monitors over-current on the USB bus (external circuitry required to detect over-current condition).
						-	**R** — Function reserved.
						I	**T2_CAP3** — Capture input 3 of timer 2.
						-	**R** — Function reserved.
						-	**R** — Function reserved.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA180	LQFP208		Reset state [1]	Type	Description
P6_7	J13	H11	123	[2]	N; PU	-	**R** — Function reserved.
						I/O	**EMC_A15** — External memory address line 15.
						-	**R** — Function reserved.
						O	**USB0_IND1** — USB0 port indicator LED control output 1.
						I/O	**GPIO5[15]** — General purpose digital input/output pin.
						O	**T2_MAT0** — Match output 0 of timer 2.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
P6_8	H13	F12	125	[2]	N; PU	-	**R** — Function reserved.
						I/O	**EMC_A14** — External memory address line 14.
						-	**R** — Function reserved.
						O	**USB0_IND0** — USB0 port indicator LED control output 0.
						I/O	**GPIO5[16]** — General purpose digital input/output pin.
						O	**T2_MAT1** — Match output 1 of timer 2.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
P6_9	J15	H13	139	[2]	N; PU	I/O	**GPIO3[5]** — General purpose digital input/output pin.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
						O	**EMC_DYCS0** — SDRAM chip select 0.
						-	**R** — Function reserved.
						O	**T2_MAT2** — Match output 2 of timer 2.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
P6_10	H15	G13	142	[2]	N; PU	I/O	**GPIO3[6]** — General purpose digital input/output pin.
						O	**MCABORT** — Motor control PWM, LOW-active fast abort.
						-	**R** — Function reserved.
						O	**EMC_DQMOUT1** — Data mask 1 used with SDRAM and static devices.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
						-	**R** — Function reserved.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA180	LQFP208		Reset state [1]	Type	Description
P6_11	H12	F11	143	[2]	N; PU	I/O	**GPIO3[7]** — General purpose digital input/output pin.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
						O	**EMC_CKEOUT0** — SDRAM clock enable 0.
						-	**R** — Function reserved.
						O	**T2_MAT3** — Match output 3 of timer 2.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
P6_12	G15	F13	145	[2]	N; PU	I/O	**GPIO2[8]** — General purpose digital input/output pin.
						O	**CTOUT_7** — SCT output 7. Match output 3 of timer 1.
						-	**R** — Function reserved.
						O	**EMC_DQMOUT0** — Data mask 0 used with SDRAM and static devices.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
P7_0	B16	B14	158	[2]	N; PU	I/O	**GPIO3[8]** — General purpose digital input/output pin.
						O	**CTOUT_14** — SCT output 14. Match output 2 of timer 3.
						-	**R** — Function reserved.
						O	**LCD_LE** — Line end signal.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
P7_1	C14	C13	162	[2]	N; PU	I/O	**GPIO3[9]** — General purpose digital input/output pin.
						O	**CTOUT_15** — SCT output 15. Match output 3 of timer 3.
						I/O	**I2S0_TX_WS** — Transmit Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I^2S-bus specification*.
						O	**LCD_VD19** — LCD data.
						O	**LCD_VD7** — LCD data.
						-	**R** — Function reserved.
						O	**U2_TXD** — Transmitter output for USART2.
						-	**R** — Function reserved.

Table 3. Pin description *...continued*

Pin name	LBGA256	TFBGA180	LQFP208		Reset state [1]	Type	Description
P7_2	A16	A14	165	[2]	N; PU	I/O	**GPIO3[10] —** General purpose digital input/output pin.
						I	**CTIN_4 —** SCT input 4. Capture input 2 of timer 1.
						I/O	**I2S0_TX_SDA —** I^2S transmit data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I^2S-bus specification*.
						O	**LCD_VD18 —** LCD data.
						O	**LCD_VD6 —** LCD data.
						-	**R —** Function reserved.
						I	**U2_RXD —** Receiver input for USART2.
						-	**R —** Function reserved.
P7_3	C13	C12	167	[2]	N; PU	I/O	**GPIO3[11] —** General purpose digital input/output pin.
						I	**CTIN_3 —** SCT input 3. Capture input 1 of timer 1.
						-	**R —** Function reserved.
						O	**LCD_VD17 —** LCD data.
						O	**LCD_VD5 —** LCD data.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
P7_4	C8	C6	189	[5]	N; PU	I/O	**GPIO3[12] —** General purpose digital input/output pin.
						O	**CTOUT_13 —** SCT output 13. Match output 3 of timer 3.
						-	**R —** Function reserved.
						O	**LCD_VD16 —** LCD data.
						O	**LCD_VD4 —** LCD data.
						O	**TRACEDATA[0] —** Trace data, bit 0.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						AI	**ADC0_4 —** ADC0, input channel 4. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA180	LQFP208		Reset state [1]	Type	Description
P7_5	A7	C7	191	[5]	N; PU	I/O	**GPIO3[13]** — General purpose digital input/output pin.
						O	**CTOUT_12** — SCT output 12. Match output 3 of timer 3.
						-	**R** — Function reserved.
						O	**LCD_VD8** — LCD data.
						O	**LCD_VD23** — LCD data.
						O	**TRACEDATA[1]** — Trace data, bit 1.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
						AI	**ADC0_3** — ADC0, input channel 3.Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC.
P7_6	C7	F5	194	[2]	N; PU	I/O	**GPIO3[14]** — General purpose digital input/output pin.
						O	**CTOUT_11** — SCT output 1. Match output 3 of timer 2.
						-	**R** — Function reserved.
						O	**LCD_LP** — Line synchronization pulse (STN). Horizontal synchronization pulse (TFT).
						-	**R** — Function reserved.
						O	**TRACEDATA[2]** — Trace data, bit 2.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
P7_7	B6	D5	201	[5]	N; PU	I/O	**GPIO3[15]** — General purpose digital input/output pin.
						O	**CTOUT_8** — SCT output 8. Match output 0 of timer 2.
						-	**R** — Function reserved.
						O	**LCD_PWR** — LCD panel power enable.
						-	**R** — Function reserved.
						O	**TRACEDATA[3]** — Trace data, bit 3.
						O	**ENET_MDC** — Ethernet MIIM clock.
						-	**R** — Function reserved.
						AI	**ADC1_6** — ADC1, input channel 6. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA180	LQFP208		Reset state [1]	Type	Description
P8_0	E5	E4	2	[3]	N; PU	I/O	**GPIO4[0]** — General purpose digital input/output pin.
						I	**USB0_PWR_FAULT** — Port power fault signal indicating overcurrent condition; this signal monitors over-current on the USB bus (external circuitry required to detect over-current condition).
						-	**R** — Function reserved.
						I	**MCI2** — Motor control PWM channel 2, input.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
						O	**T0_MAT0** — Match output 0 of timer 0.
P8_1	H5	G4	34	[3]	N; PU	I/O	**GPIO4[1]** — General purpose digital input/output pin.
						O	**USB0_IND1** — USB0 port indicator LED control output 1.
						-	**R** — Function reserved.
						I	**MCI1** — Motor control PWM channel 1, input.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
						O	**T0_MAT1** — Match output 1 of timer 0.
P8_2	K4	J4	36	[3]	N; PU	I/O	**GPIO4[2]** — General purpose digital input/output pin.
						O	**USB0_IND0** — USB0 port indicator LED control output 0.
						-	**R** — Function reserved.
						I	**MCI0** — Motor control PWM channel 0, input.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
						O	**T0_MAT2** — Match output 2 of timer 0.
P8_3	J3	H3	37	[2]	N; PU	I/O	**GPIO4[3]** — General purpose digital input/output pin.
						I/O	**USB1_ULPI_D2** — ULPI link bidirectional data line 2.
						-	**R** — Function reserved.
						O	**LCD_VD12** — LCD data.
						O	**LCD_VD19** — LCD data.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
						O	**T0_MAT3** — Match output 3 of timer 0.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA180	LQFP208		Reset state [1]	Type	Description
P8_4	J2	H2	39	[2]	N; PU	I/O	**GPIO4[4]** — General purpose digital input/output pin.
						I/O	**USB1_ULPI_D1** — ULPI link bidirectional data line 1.
						-	**R** — Function reserved.
						O	**LCD_VD7** — LCD data.
						O	**LCD_VD16** — LCD data.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
						I	**T0_CAP0** — Capture input 0 of timer 0.
P8_5	J1	H1	40	[2]	N; PU	I/O	**GPIO4[5]** — General purpose digital input/output pin.
						I/O	**USB1_ULPI_D0** — ULPI link bidirectional data line 0.
						-	**R** — Function reserved.
						O	**LCD_VD6** — LCD data.
						O	**LCD_VD8** — LCD data.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
						I	**T0_CAP1** — Capture input 1 of timer 0.
P8_6	K3	J3	43	[2]	N; PU	I/O	**GPIO4[6]** — General purpose digital input/output pin.
						I	**USB1_ULPI_NXT** — ULPI link NXT signal. Data flow control signal from the PHY.
						-	**R** — Function reserved.
						O	**LCD_VD5** — LCD data.
						O	**LCD_LP** — Line synchronization pulse (STN). Horizontal synchronization pulse (TFT).
						-	**R** — Function reserved.
						-	**R** — Function reserved.
						I	**T0_CAP2** — Capture input 2 of timer 0.
P8_7	K1	J1	45	[2]	N; PU	I/O	**GPIO4[7]** — General purpose digital input/output pin.
						O	**USB1_ULPI_STP** — ULPI link STP signal. Asserted to end or interrupt transfers to the PHY.
						-	**R** — Function reserved.
						O	**LCD_VD4** — LCD data.
						O	**LCD_PWR** — LCD panel power enable.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
						I	**T0_CAP3** — Capture input 3 of timer 0.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA180	LQFP208		Reset state [1]	Type	Description
P8_8	L1	K1	49	[2]	N; PU	-	**R** — Function reserved.
						I	**USB1_ULPI_CLK** — ULPI link CLK signal. 60 MHz clock generated by the PHY.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
						O	**CGU_OUT0** — CGU spare clock output 0.
						O	**I2S1_TX_MCLK** — I^{2}S1 transmit master clock.
P9_0	T1	P1	59	[2]	N; PU	I/O	**GPIO4[12]** — General purpose digital input/output pin.
						O	**$\overline{\text{MCABORT}}$** — Motor control PWM, LOW-active fast abort.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
						I	**ENET_CRS** — Ethernet Carrier Sense (MII interface).
						-	**R** — Function reserved.
						I/O	**SSP0_SSEL** — Slave Select for SSP0.
P9_1	N6	P4	66	[2]	N; PU	I/O	**GPIO4[13]** — General purpose digital input/output pin.
						O	**MCOA2** — Motor control PWM channel 2, output A.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
						I/O	**I2S0_TX_WS** — Transmit Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I^{2}S-bus specification*.
						I	**ENET_RX_ER** — Ethernet receive error (MII interface).
						-	**R** — Function reserved.
						I/O	**SSP0_MISO** — Master In Slave Out for SSP0.
P9_2	N8	M6	70	[2]	N; PU	I/O	**GPIO4[14]** — General purpose digital input/output pin.
						O	**MCOB2** — Motor control PWM channel 2, output B.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
						I/O	**I2S0_TX_SDA** — I^{2}S transmit data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I^{2}S-bus specification*.
						I	**ENET_RXD3** — Ethernet receive data 3 (MII interface).
						-	**R** — Function reserved.
						I/O	**SSP0_MOSI** — Master Out Slave in for SSP0.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA180	LQFP208		Reset state [1]	Type	Description
P9_3	M6	P5	79	[2]	N; PU	I/O	**GPIO4[15]** — General purpose digital input/output pin.
						O	**MCOA0** — Motor control PWM channel 0, output A.
						O	**USB1_IND1** — USB1 Port indicator LED control output 1.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
						I	**ENET_RXD2** — Ethernet receive data 2 (MII interface).
						-	**R** — Function reserved.
						O	**U3_TXD** — Transmitter output for USART3.
P9_4	N10	M8	92	[2]	N; PU	-	**R** — Function reserved.
						O	**MCOB0** — Motor control PWM channel 0, output B.
						O	**USB1_IND0** — USB1 Port indicator LED control output 0.
						-	**R** — Function reserved.
						I/O	**GPIO5[17]** — General purpose digital input/output pin.
						O	**ENET_TXD2** — Ethernet transmit data 2 (MII interface).
						-	**R** — Function reserved.
						I	**U3_RXD** — Receiver input for USART3.
P9_5	M9	L7	98	[2]	N; PU	-	**R** — Function reserved.
						O	**MCOA1** — Motor control PWM channel 1, output A.
						O	**USB1_PPWR** — VBUS drive signal (towards external charge pump or power management unit); indicates that VBUS must be driven (active HIGH). Add a pull-down resistor to disable the power switch at reset. This signal has opposite polarity compared to the USB_PPWR used on other NXP LPC parts.
						-	**R** — Function reserved.
						I/O	**GPIO5[18]** — General purpose digital input/output pin.
						O	**ENET_TXD3** — Ethernet transmit data 3 (MII interface).
						-	**R** — Function reserved.
						O	**U0_TXD** — Transmitter output for USART0.
P9_6	L11	M9	103	[2]	N; PU	I/O	**GPIO4[11]** — General purpose digital input/output pin.
						O	**MCOB1** — Motor control PWM channel 1, output B.
						I	**USB1_PWR_FAULT** — USB1 Port power fault signal indicating over-current condition; this signal monitors over-current on the USB1 bus (external circuitry required to detect over-current condition).
						-	**R** — Function reserved.
						-	**R** — Function reserved.
						I	**ENET_COL** — Ethernet Collision detect (MII interface).
						-	**R** — Function reserved.
						I	**U0_RXD** — Receiver input for USART0.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA180	LQFP208		Reset state [1]	Type	Description
PA_0	L12	L10	126	[2]	N; PU	-	**R** — Function reserved.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
						O	**I2S1_RX_MCLK** — I^{2}S1 receive master clock.
						O	**CGU_OUT1** — CGU spare clock output 1.
						-	**R** — Function reserved.
PA_1	J14	H12	134	[3]	N; PU	I/O	**GPIO4[8]** — General purpose digital input/output pin.
						I	**QEI_IDX** — Quadrature Encoder Interface INDEX input.
						-	**R** — Function reserved.
						O	**U2_TXD** — Transmitter output for USART2.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
PA_2	K15	J13	136	[3]	N; PU	I/O	**GPIO4[9]** — General purpose digital input/output pin.
						I	**QEI_PHB** — Quadrature Encoder Interface PHB input.
						-	**R** — Function reserved.
						I	**U2_RXD** — Receiver input for USART2.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
PA_3	H11	E10	147	[3]	N; PU	I/O	**GPIO4[10]** — General purpose digital input/output pin.
						I	**QEI_PHA** — Quadrature Encoder Interface PHA input.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
						-	**R** — Function reserved.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA180	LQFP208		Reset state [1]	Type	Description
PA_4	G13	E12	151	[2]	N; PU	-	**R** — Function reserved.
						O	**CTOUT_9** — SCT output 9. Match output 3 of timer 3.
						-	**R** — Function reserved.
						I/O	**EMC_A23** — External memory address line 23.
						I/O	**GPIO5[19]** — General purpose digital input/output pin.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
PB_0	B15	D14	164	[2]	N; PU	-	**R** — Function reserved.
						O	**CTOUT_10** — SCT output 10. Match output 3 of timer 3.
						O	**LCD_VD23** — LCD data.
						-	**R** — Function reserved.
						I/O	**GPIO5[20]** — General purpose digital input/output pin.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
PB_1	A14	A13	175	[2]	N; PU	-	**R** — Function reserved.
						I	**USB1_ULPI_DIR** — ULPI link DIR signal. Controls the ULP data line direction.
						O	**LCD_VD22** — LCD data.
						-	**R** — Function reserved.
						I/O	**GPIO5[21]** — General purpose digital input/output pin.
						O	**CTOUT_6** — SCT output 6. Match output 2 of timer 1.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
PB_2	B12	B11	177	[2]	N; PU	-	**R** — Function reserved.
						I/O	**USB1_ULPI_D7** — ULPI link bidirectional data line 7.
						O	**LCD_VD21** — LCD data.
						-	**R** — Function reserved.
						I/O	**GPIO5[22]** — General purpose digital input/output pin.
						O	**CTOUT_7** — SCT output 7. Match output 3 of timer 1.
						-	**R** — Function reserved.
						-	**R** — Function reserved.

Table 3. Pin description …continued

Pin name	LBGA256	TFBGA180	LQFP208		Reset state [1]	Type	Description
PB_3	A13	A12	178	[2]	N; PU	-	**R** — Function reserved.
						I/O	**USB1_ULPI_D6** — ULPI link bidirectional data line 6.
						O	**LCD_VD20** — LCD data.
						-	**R** — Function reserved.
						I/O	**GPIO5[23]** — General purpose digital input/output pin.
						O	**CTOUT_8** — SCT output 8. Match output 0 of timer 2.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
PB_4	B11	B10	180	[2]	N; PU	-	**R** — Function reserved.
						I/O	**USB1_ULPI_D5** — ULPI link bidirectional data line 5.
						O	**LCD_VD15** — LCD data.
						-	**R** — Function reserved.
						I/O	**GPIO5[24]** — General purpose digital input/output pin.
						I	**CTIN_5** — SCT input 5. Capture input 2 of timer 2.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
PB_5	A12	A11	181	[2]	N; PU	-	**R** — Function reserved.
						I/O	**USB1_ULPI_D4** — ULPI link bidirectional data line 4.
						O	**LCD_VD14** — LCD data.
						-	**R** — Function reserved.
						I/O	**GPIO5[25]** — General purpose digital input/output pin.
						I	**CTIN_7** — SCT input 7.
						O	**LCD_PWR** — LCD panel power enable.
						-	**R** — Function reserved.
PB_6	A6	C5	-	[5]	N; PU	-	**R** — Function reserved.
						I/O	**USB1_ULPI_D3** — ULPI link bidirectional data line 3.
						O	**LCD_VD13** — LCD data.
						-	**R** — Function reserved.
						I/O	**GPIO5[26]** — General purpose digital input/output pin.
						I	**CTIN_6** — SCT input 6. Capture input 1 of timer 3.
						O	**LCD_VD19** — LCD data.
						-	**R** — Function reserved.
						AI	**ADC0_6** — ADC0, input channel 6. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA180	LQFP208		Reset state [1]	Type	Description
PC_0	D4	-	7	[5]	N; PU	-	**R** — Function reserved.
						I	**USB1_ULPI_CLK** — ULPI link CLK signal. 60 MHz clock generated by the PHY.
						-	**R** — Function reserved.
						I/O	**ENET_RX_CLK** — Ethernet Receive Clock (MII interface).
						O	**LCD_DCLK** — LCD panel clock.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
						I/O	**SD_CLK** — SD/MMC card clock.
						AI	**ADC1_1** — ADC1, input channel 1. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC.
PC_1	E4	-	9	[2]	N; PU	I/O	**USB1_ULPI_D7** — ULPI link bidirectional data line 7.
						-	**R** — Function reserved.
						I	**U1_RI** — Ring Indicator input for UART1.
						O	**ENET_MDC** — Ethernet MIIM clock.
						I/O	**GPIO6[0]** — General purpose digital input/output pin.
						-	**R** — Function reserved.
						I	**T3_CAP0** — Capture input 0 of timer 3.
						O	**SD_VOLT0** — SD/MMC bus voltage select output 0.
PC_2	F6	-	13	[2]	N; PU	I/O	**USB1_ULPI_D6** — ULPI link bidirectional data line 6.
						-	**R** — Function reserved.
						I	**U1_CTS** — Clear to Send input for UART1.
						O	**ENET_TXD2** — Ethernet transmit data 2 (MII interface).
						I/O	**GPIO6[1]** — General purpose digital input/output pin.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
						O	**SD_RST** — SD/MMC reset signal for MMC4.4 card.
PC_3	F5	-	11	[5]	N; PU	I/O	**USB1_ULPI_D5** — ULPI link bidirectional data line 5.
						-	**R** — Function reserved.
						O	**U1_RTS** — Request to Send output for UART1. Can also be configured to be an RS-485/EIA-485 output enable signal for UART1.
						O	**ENET_TXD3** — Ethernet transmit data 3 (MII interface).
						I/O	**GPIO6[2]** — General purpose digital input/output pin.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
						O	**SD_VOLT1** — SD/MMC bus voltage select output 1.
						AI	**ADC1_0** — ADC1, input channel 0. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA180	LQFP208		Reset state [1]	Type	Description
PC_4	F4	-	16	[2]	N; PU	-	**R —** Function reserved.
						I/O	**USB1_ULPI_D4 —** ULPI link bidirectional data line 4.
						-	**R —** Function reserved.
							ENET_TX_EN — Ethernet transmit enable (RMII/MII interface).
						I/O	**GPIO6[3] —** General purpose digital input/output pin.
						-	**R —** Function reserved.
						I	**T3_CAP1 —** Capture input 1 of timer 3.
						I/O	**SD_DAT0 —** SD/MMC data bus line 0.
PC_5	G4	-	20	[2]	N; PU	-	**R —** Function reserved.
						I/O	**USB1_ULPI_D3 —** ULPI link bidirectional data line 3.
						-	**R —** Function reserved.
						O	**ENET_TX_ER —** Ethernet Transmit Error (MII interface).
						I/O	**GPIO6[4] —** General purpose digital input/output pin.
						-	**R —** Function reserved.
						I	**T3_CAP2 —** Capture input 2 of timer 3.
						I/O	**SD_DAT1 —** SD/MMC data bus line 1.
PC_6	H6	-	22	[2]	N; PU	-	**R —** Function reserved.
						I/O	**USB1_ULPI_D2 —** ULPI link bidirectional data line 2.
						-	**R —** Function reserved.
						I	**ENET_RXD2 —** Ethernet receive data 2 (MII interface).
						I/O	**GPIO6[5] —** General purpose digital input/output pin.
						-	**R —** Function reserved.
						I	**T3_CAP3 —** Capture input 3 of timer 3.
						I/O	**SD_DAT2 —** SD/MMC data bus line 2.
PC_7	G5	-	-	[2]	N; PU	-	**R —** Function reserved.
						I/O	**USB1_ULPI_D1 —** ULPI link bidirectional data line 1.
						-	**R —** Function reserved.
						I	**ENET_RXD3 —** Ethernet receive data 3 (MII interface).
						I/O	**GPIO6[6] —** General purpose digital input/output pin.
						-	**R —** Function reserved.
						O	**T3_MAT0 —** Match output 0 of timer 3.
						I/O	**SD_DAT3 —** SD/MMC data bus line 3.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA180	LQFP208		Reset state [1]	Type	Description
PC_8	N4	-	-	[2]	N; PU	-	**R** — Function reserved.
						I/O	**USB1_ULPI_D0** — ULPI link bidirectional data line 0.
						-	**R** — Function reserved.
						I	**ENET_RX_DV** — Ethernet Receive Data Valid (RMII/MII interface).
						I/O	**GPIO6[7]** — General purpose digital input/output pin.
						-	**R** — Function reserved.
						O	**T3_MAT1** — Match output 1 of timer 3.
						I	**SD_CD** — SD/MMC card detect input.
PC_9	K2	-	-	[2]	N; PU	-	**R** — Function reserved.
						I	**USB1_ULPI_NXT** — ULPI link NXT signal. Data flow control signal from the PHY.
						-	**R** — Function reserved.
						I	**ENET_RX_ER** — Ethernet receive error (MII interface).
						I/O	**GPIO6[8]** — General purpose digital input/output pin.
						-	**R** — Function reserved.
						O	**T3_MAT2** — Match output 2 of timer 3.
						O	**SD_POW** — SD/MMC power monitor output.
PC_10	M5	-	-	[2]	N; PU	-	**R** — Function reserved.
						O	**USB1_ULPI_STP** — ULPI link STP signal. Asserted to end or interrupt transfers to the PHY.
						I	**U1_DSR** — Data Set Ready input for UART1.
						-	**R** — Function reserved.
						I/O	**GPIO6[9]** — General purpose digital input/output pin.
						-	**R** — Function reserved.
						O	**T3_MAT3** — Match output 3 of timer 3.
						I/O	**SD_CMD** — SD/MMC command signal.
PC_11	L5	-	-	[2]	N; PU	-	**R** — Function reserved.
						I	**USB1_ULPI_DIR** — ULPI link DIR signal. Controls the ULP data line direction.
						I	**U1_DCD** — Data Carrier Detect input for UART1.
						-	**R** — Function reserved.
						I/O	**GPIO6[10]** — General purpose digital input/output pin.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
						I/O	**SD_DAT4** — SD/MMC data bus line 4.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA180	LQFP208		Reset state [1]	Type	Description
PC_12	L6	-	-	[2]	N; PU	-	**R —** Function reserved.
						-	**R —** Function reserved.
						O	**U1_DTR —** Data Terminal Ready output for UART1. Can also be configured to be an RS-485/EIA-485 output enable signal for UART1.
						-	**R —** Function reserved.
						I/O	**GPIO6[11] —** General purpose digital input/output pin.
						-	**R —** Function reserved.
						I/O	**I2S0_TX_SDA —** I^2S transmit data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I^2S-bus specification*.
						I/O	**SD_DAT5 —** SD/MMC data bus line 5.
PC_13	M1	-	-	[2]	N; PU	-	**R —** Function reserved.
						-	**R —** Function reserved.
						O	**U1_TXD —** Transmitter output for UART1.
						-	**R —** Function reserved.
						I/O	**GPIO6[12] —** General purpose digital input/output pin.
						-	**R —** Function reserved.
						I/O	**I2S0_TX_WS —** Transmit Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I^2S-bus specification*.
						I/O	**SD_DAT6 —** SD/MMC data bus line 6.
PC_14	N1	-	-	[2]	N; PU	-	**R —** Function reserved.
						-	**R —** Function reserved.
						I	**U1_RXD —** Receiver input for UART1.
						-	**R —** Function reserved.
						I/O	**GPIO6[13] —** General purpose digital input/output pin.
						-	**R —** Function reserved.
						O	**ENET_TX_ER —** Ethernet Transmit Error (MII interface).
						I/O	**SD_DAT7 —** SD/MMC data bus line 7.
PD_0	N2	-	-	[2]	N; PU	-	**R —** Function reserved.
						O	**CTOUT_15 —** SCT output 15. Match output 3 of timer 3.
						O	**EMC_DQMOUT2 —** Data mask 2 used with SDRAM and static devices.
						-	**R —** Function reserved.
						I/O	**GPIO6[14] —** General purpose digital input/output pin.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						-	**R —** Function reserved.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA180	LQFP208		Reset state [1]	Type	Description
PD_1	P1	-	-	[2]	N; PU	-	**R** — Function reserved.
						-	**R** — Function reserved.
						O	**EMC_CKEOUT2** — SDRAM clock enable 2.
						-	**R** — Function reserved.
						I/O	**GPIO6[15]** — General purpose digital input/output pin.
						O	**SD_POW** — SD/MMC power monitor output.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
PD_2	R1	-	-	[2]	N; PU	-	**R** — Function reserved.
						O	**CTOUT_7** — SCT output 7. Match output 3 of timer 1.
						I/O	**EMC_D16** — External memory data line 16.
						-	**R** — Function reserved.
						I/O	**GPIO6[16]** — General purpose digital input/output pin.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
PD_3	P4	-	-	[2]	N; PU	-	**R** — Function reserved.
						O	**CTOUT_6** — SCT output 7. Match output 2 of timer 1.
						I/O	**EMC_D17** — External memory data line 17.
						-	**R** — Function reserved.
						I/O	**GPIO6[17]** — General purpose digital input/output pin.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
PD_4	T2	-	-	[2]	N; PU	-	**R** — Function reserved.
						O	**CTOUT_8** — SCT output 8. Match output 0 of timer 2.
						I/O	**EMC_D18** — External memory data line 18.
						-	**R** — Function reserved.
						I/O	**GPIO6[18]** — General purpose digital input/output pin.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
						-	**R** — Function reserved.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA180	LQFP208		Reset state [1]	Type	Description
PD_5	P6	-	-	[2]	N; PU	-	**R —** Function reserved.
						O	**CTOUT_9 —** SCT output 9. Match output 3 of timer 3.
						I/O	**EMC_D19 —** External memory data line 19.
						-	**R —** Function reserved.
						I/O	**GPIO6[19] —** General purpose digital input/output pin.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
PD_6	R6	-	68	[2]	N; PU	-	**R —** Function reserved.
						O	**CTOUT_10 —** SCT output 10. Match output 3 of timer 3.
						I/O	**EMC_D20 —** External memory data line 20.
						-	**R —** Function reserved.
						I/O	**GPIO6[20] —** General purpose digital input/output pin.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
PD_7	T6	-	72	[2]	N; PU	-	**R —** Function reserved.
						I	**CTIN_5 —** SCT input 5. Capture input 2 of timer 2.
						I/O	**EMC_D21 —** External memory data line 21.
						-	**R —** Function reserved.
						I/O	**GPIO6[21] —** General purpose digital input/output pin.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
PD_8	P8	-	74	[2]	N; PU	-	**R —** Function reserved.
						I	**CTIN_6 —** SCT input 6. Capture input 1 of timer 3.
						I/O	**EMC_D22 —** External memory data line 22.
						-	**R —** Function reserved.
						I/O	**GPIO6[22] —** General purpose digital input/output pin.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						-	**R —** Function reserved.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA180	LQFP208		Reset state [1]	Type	Description
PD_9	T11	-	84	[2]	N; PU	-	**R —** Function reserved.
						O	**CTOUT_13 —** SCT output 13. Match output 3 of timer 3.
						I/O	**EMC_D23 —** External memory data line 23.
						-	**R —** Function reserved.
						I/O	**GPIO6[23] —** General purpose digital input/output pin.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
PD_10	P11	-	86	[2]	N; PU	-	**R —** Function reserved.
						I	**CTIN_1 —** SCT input 1. Capture input 1 of timer 0. Capture input 1 of timer 2.
						O	**$\overline{\mathrm{EMC\_BLS3}}$ —** LOW active Byte Lane select signal 3.
						-	**R —** Function reserved.
						I/O	**GPIO6[24] —** General purpose digital input/output pin.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
PD_11	N9	M7	88	[2]	N; PU	-	**R —** Function reserved.
						-	**R —** Function reserved.
						O	**$\overline{\mathrm{EMC\_CS3}}$ —** LOW active Chip Select 3 signal.
						-	**R —** Function reserved.
						I/O	**GPIO6[25] —** General purpose digital input/output pin.
						I/O	**USB1_ULPI_D0 —** ULPI link bidirectional data line 0.
						O	**CTOUT_14 —** SCT output 14. Match output 2 of timer 3.
						-	**R —** Function reserved.
PD_12	N11	P9	94	[2]	N; PU	-	**R —** Function reserved.
						-	**R —** Function reserved.
						O	**$\overline{\mathrm{EMC\_CS2}}$ —** LOW active Chip Select 2 signal.
						-	**R —** Function reserved.
						I/O	**GPIO6[26] —** General purpose digital input/output pin.
						-	**R —** Function reserved.
						O	**CTOUT_10 —** SCT output 10. Match output 3 of timer 3.
						-	**R —** Function reserved.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA180	LQFP208		Reset state [1]	Type	Description
PD_13	T14	-	97	[2]	N; PU	-	**R** — Function reserved.
						I	**CTIN_0** — SCT input 0. Capture input 0 of timer 0, 1, 2, 3.
						O	**EMC_BLS2** — LOW active Byte Lane select signal 2.
						-	**R** — Function reserved.
						I/O	**GPIO6[27]** — General purpose digital input/output pin.
						-	**R** — Function reserved.
						O	**CTOUT_13** — SCT output 13. Match output 3 of timer 3.
						-	**R** — Function reserved.
PD_14	R13	L11	99	[2]	N; PU	-	**R** — Function reserved.
						-	**R** — Function reserved.
						O	**EMC_DYCS2** — SDRAM chip select 2.
						-	**R** — Function reserved.
						I/O	**GPIO6[28]** — General purpose digital input/output pin.
						-	**R** — Function reserved.
						O	**CTOUT_11** — SCT output 11. Match output 3 of timer 2.
						-	**R** — Function reserved.
PD_15	T15	P13	101	[2]	N; PU	-	**R** — Function reserved.
						-	**R** — Function reserved.
						I/O	**EMC_A17** — External memory address line 17.
						-	**R** — Function reserved.
						I/O	**GPIO6[29]** — General purpose digital input/output pin.
						I	**SD_WP** — SD/MMC card write protect input.
						O	**CTOUT_8** — SCT output 8. Match output 0 of timer 2.
						-	**R** — Function reserved.
PD_16	R14	P12	104	[2]	N; PU	-	**R** — Function reserved.
						-	**R** — Function reserved.
						I/O	**EMC_A16** — External memory address line 16.
						-	**R** — Function reserved.
						I/O	**GPIO6[30]** — General purpose digital input/output pin.
						O	**SD_VOLT2** — SD/MMC bus voltage select output 2.
						O	**CTOUT_12** — SCT output 12. Match output 3 of timer 3.
						-	**R** — Function reserved.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA180	LQFP208		Reset state [1]	Type	Description
PE_0	P14	N12	106	[2]	N; PU	-	**R** — Function reserved.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
						I/O	**EMC_A18** — External memory address line 18.
						I/O	**GPIO7[0]** — General purpose digital input/output pin.
						O	**CAN1_TD** — CAN1 transmitter output.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
PE_1	N14	M12	112	[2]	N; PU	-	**R** — Function reserved.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
						I/O	**EMC_A19** — External memory address line 19.
						I/O	**GPIO7[1]** — General purpose digital input/output pin.
						I	**CAN1_RD** — CAN1 receiver input.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
PE_2	M14	L12	115	[2]	N; PU	I	**ADCTRIG0** — ADC trigger input 0.
						I	**CAN0_RD** — CAN receiver input.
						-	**R** — Function reserved.
						I/O	**EMC_A20** — External memory address line 20.
						I/O	**GPIO7[2]** — General purpose digital input/output pin.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
PE_3	K12	K10	118	[2]	N; PU	-	**R** — Function reserved.
						O	**CAN0_TD** — CAN transmitter output.
						I	**ADCTRIG1** — ADC trigger input 1.
						I/O	**EMC_A21** — External memory address line 21.
						I/O	**GPIO7[3]** — General purpose digital input/output pin.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
						-	**R** — Function reserved.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA180	LQFP208		Reset state [1]	Type	Description
PE_4	K13	J11	120	[2]	N; PU	-	**R** — Function reserved.
						I	**NMI** — External interrupt input to NMI.
						-	**R** — Function reserved.
						I/O	**EMC_A22** — External memory address line 22.
						I/O	**GPIO7[4]** — General purpose digital input/output pin.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
PE_5	N16	-	122	[2]	N; PU	-	**R** — Function reserved.
						O	**CTOUT_3** — SCT output 3. Match output 3 of timer 0.
						O	**U1_RTS** — Request to Send output for UART1. Can also be configured to be an RS-485/EIA-485 output enable signal for UART1.
						I/O	**EMC_D24** — External memory data line 24.
						I/O	**GPIO7[5]** — General purpose digital input/output pin.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
PE_6	M16	-	124	[2]	N; PU	-	**R** — Function reserved.
						O	**CTOUT_2** — SCT output 2. Match output 2 of timer 0.
						I	**U1_RI** — Ring Indicator input for UART1.
						I/O	**EMC_D25** — External memory data line 25.
						I/O	**GPIO7[6]** — General purpose digital input/output pin.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
PE_7	F15	-	149	[2]	N; PU	-	**R** — Function reserved.
						O	**CTOUT_5** — SCT output 5. Match output 3 of timer 3.
						I	**U1_CTS** — Clear to Send input for UART1.
						I/O	**EMC_D26** — External memory data line 26.
						I/O	**GPIO7[7]** — General purpose digital input/output pin.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
						-	**R** — Function reserved.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA180	LQFP208		Reset state [1]	Type	Description
PE_8	F14	-	150	[2]	N; PU	-	**R —** Function reserved.
						O	**CTOUT_4 —** SCT output 4. Match output 3 of timer 3.
						I	**U1_DSR —** Data Set Ready input for UART1.
						I/O	**EMC_D27 —** External memory data line 27.
						I/O	**GPIO7[8] —** General purpose digital input/output pin.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
PE_9	E16	-	152	[2]	N; PU	-	**R —** Function reserved.
						I	**CTIN_4 —** SCT input 4. Capture input 2 of timer 1.
						I	**U1_DCD —** Data Carrier Detect input for UART1.
						I/O	**EMC_D28 —** External memory data line 28.
						I/O	**GPIO7[9] —** General purpose digital input/output pin.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
PE_10	E14	-	154	[2]	N; PU	-	**R —** Function reserved.
						I	**CTIN_3 —** SCT input 3. Capture input 1 of timer 1.
						O	**U1_DTR —** Data Terminal Ready output for UART1. Can also be configured to be an RS-485/EIA-485 output enable signal for UART1.
						I/O	**EMC_D29 —** External memory data line 29.
						I/O	**GPIO7[10] —** General purpose digital input/output pin.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
PE_11	D16	-	-	[2]	N; PU	-	**R —** Function reserved.
						O	**CTOUT_12 —** SCT output 12. Match output 3 of timer 3.
						O	**U1_TXD —** Transmitter output for UART1.
						I/O	**EMC_D30 —** External memory data line 30.
						I/O	**GPIO7[11] —** General purpose digital input/output pin.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						-	**R —** Function reserved.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA180	LQFP208		Reset state [1]	Type	Description
PE_12	D15	-	-	[2]	N; PU	-	**R** — Function reserved.
						O	**CTOUT_11** — SCT output 11. Match output 3 of timer 2.
						I	**U1_RXD** — Receiver input for UART1.
						I/O	**EMC_D31** — External memory data line 31.
						I/O	**GPIO7[12]** — General purpose digital input/output pin.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
PE_13	G14	-	-	[2]	N; PU	-	**R** — Function reserved.
						O	**CTOUT_14** — SCT output 14. Match output 2 of timer 3.
						I/O	**I2C1_SDA** — I^{2}C1 data input/output (this pin does not use a specialized I^{2}C pad).
						O	**EMC_DQMOUT3** — Data mask 3 used with SDRAM and static devices.
						I/O	**GPIO7[13]** — General purpose digital input/output pin.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
PE_14	C15	-	-	[2]	N; PU	-	**R** — Function reserved.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
						O	**EMC_DYCS3** — SDRAM chip select 3.
						I/O	**GPIO7[14]** — General purpose digital input/output pin.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
PE_15	E13	-	-	[2]	N; PU	-	**R** — Function reserved.
						O	**CTOUT_0** — SCT output 0. Match output 0 of timer 0.
						I/O	**I2C1_SCL** — I^{2}C1 clock input/output (this pin does not use a specialized I^{2}C pad).
						O	**EMC_CKEOUT3** — SDRAM clock enable 3.
						I/O	**GPIO7[15]** — General purpose digital input/output pin.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
						-	**R** — Function reserved.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA180	LQFP208		Reset state [1]	Type	Description
PF_0	D12	-	159	[2]	OL; PU	I/O	**SSP0_SCK** — Serial clock for SSP0.
						I	**GP_CLKIN** — General purpose clock input to the CGU.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
						O	**I2S1_TX_MCLK** — I^{2}S1 transmit master clock.
PF_1	E11	-	-	[2]	N; PU	-	**R** — Function reserved.
						-	**R** — Function reserved.
						I/O	**SSP0_SSEL** — Slave Select for SSP0.
						-	**R** — Function reserved.
						I/O	**GPIO7[16]** — General purpose digital input/output pin.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
PF_2	D11	-	168	[2]	N; PU	-	**R** — Function reserved.
						O	**U3_TXD** — Transmitter output for USART3.
						I/O	**SSP0_MISO** — Master In Slave Out for SSP0.
						-	**R** — Function reserved.
						I/O	**GPIO7[17]** — General purpose digital input/output pin.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
PF_3	E10	-	170	[2]	N; PU	-	**R** — Function reserved.
						I	**U3_RXD** — Receiver input for USART3.
						I/O	**SSP0_MOSI** — Master Out Slave in for SSP0.
						-	**R** — Function reserved.
						I/O	**GPIO7[18]** — General purpose digital input/output pin.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
						-	**R** — Function reserved.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA180	LQFP208		Reset state [1]	Type	Description
PF_4	D10	L8	172	[2]	OL; PU	I/O	**SSP1_SCK —** Serial clock for SSP1.
						I	**GP_CLKIN —** General purpose clock input to the CGU.
						O	**TRACECLK —** Trace clock.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						O	**I2S0_TX_MCLK —** I^2S transmit master clock.
						I/O	**I2S0_RX_SCK —** I^2S receive clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the *I^2S-bus specification*.
PF_5	E9	-	190	[5]	N; PU	-	**R —** Function reserved.
						I/O	**U3_UCLK —** Serial clock input/output for USART3 in synchronous mode.
						I/O	**SSP1_SSEL —** Slave Select for SSP1.
						O	**TRACEDATA[0] —** Trace data, bit 0.
						I/O	**GPIO7[19] —** General purpose digital input/output pin.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						AI	**ADC1_4 —** ADC1, input channel 4. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC.
PF_6	E7	-	192	[5]	N; PU	-	**R —** Function reserved.
						I/O	**U3_DIR —** RS-485/EIA-485 output enable/direction control for USART3.
						I/O	**SSP1_MISO —** Master In Slave Out for SSP1.
						O	**TRACEDATA[1] —** Trace data, bit 1.
						I/O	**GPIO7[20] —** General purpose digital input/output pin.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						I/O	**I2S1_TX_SDA —** I^2S1 transmit data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I^2S-bus specification*.
						AI	**ADC1_3 —** ADC1, input channel 3. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA180	LQFP208		Reset state [1]	Type	Description
PF_7	B7	-	193	[5]	N; PU	-	**R —** Function reserved.
						I/O	**U3_BAUD —** Baud pin USART3.
						I/O	**SSP1_MOSI —** Master Out Slave in for SSP1.
						O	**TRACEDATA[2] —** Trace data, bit 2.
						I/O	**GPIO7[21] —** General purpose digital input/output pin.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						I/O	**I2S1_TX_WS —** Transmit Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I^{2}S-bus specification*.
						AI/O	**ADC1_7 —** ADC1, input channel 7 or band gap output. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC.
PF_8	E6	-	-	[5]	N; PU	-	**R —** Function reserved.
						I/O	**U0_UCLK —** Serial clock input/output for USART0 in synchronous mode.
						I	**CTIN_2 —** SCT input 2. Capture input 2 of timer 0.
						O	**TRACEDATA[3] —** Trace data, bit 3.
						I/O	**GPIO7[22] —** General purpose digital input/output pin.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						AI	**ADC0_2 —** ADC0, input channel 2. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC.
PF_9	D6	-	203	[5]	N; PU	-	**R —** Function reserved.
						I/O	**U0_DIR —** RS-485/EIA-485 output enable/direction control for USART0.
						O	**CTOUT_1 —** SCT output 1. Match output 3 of timer 3.
						-	**R —** Function reserved.
						I/O	**GPIO7[23] —** General purpose digital input/output pin.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						AI	**ADC1_2 —** ADC1, input channel 2. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA180	LQFP208		Reset state [1]	Type	Description
PF_10	A3	-	205	[5]	N; PU	-	**R** — Function reserved.
						O	**U0_TXD** — Transmitter output for USART0.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
						I/O	**GPIO7[24]** — General purpose digital input/output pin.
						-	**R** — Function reserved.
						I	**SD_WP** — SD/MMC card write protect input.
						-	**R** — Function reserved.
						AI	**ADC0_5** — ADC0, input channel 5. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC.
PF_11	A2	-	207	[5]	N; PU	-	**R** — Function reserved.
						I	**U0_RXD** — Receiver input for USART0.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
						I/O	**GPIO7[25]** — General purpose digital input/output pin.
						-	**R** — Function reserved.
						O	**SD_VOLT2** — SD/MMC bus voltage select output 2.
						-	**R** — Function reserved.
						AI	**ADC1_5** — ADC1, input channel 5. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC.
Clock pins							
CLK0	N5	M4	62	[4]	O; PU	O	**EMC_CLK0** — SDRAM clock 0.
						O	**CLKOUT** — Clock output pin.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
						I/O	**SD_CLK** — SD/MMC card clock.
						O	**EMC_CLK01** — SDRAM clock 0 and clock 1 combined.
						I/O	**SSP1_SCK** — Serial clock for SSP1.
						I	**ENET_TX_CLK (ENET_REF_CLK)** — Ethernet Transmit Clock (MII interface) or Ethernet Reference Clock (RMII interface).
CLK1	T10	-	-	[4]	O; PU	O	**EMC_CLK1** — SDRAM clock 1.
						O	**CLKOUT** — Clock output pin.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
						-	**R** — Function reserved.
						O	**CGU_OUT0** — CGU spare clock output 0.
						-	**R** — Function reserved.
						O	**I2S1_TX_MCLK** — I^{2}S1 transmit master clock.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA180	LQFP208		Reset state [1]	Type	Description
CLK2	D14	P10	141	[4]	O; PU	O	**EMC_CLK3 —** SDRAM clock 3.
						O	**CLKOUT —** Clock output pin.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						I/O	**SD_CLK —** SD/MMC card clock.
						O	**EMC_CLK23 —** SDRAM clock 2 and clock 3 combined.
						O	**I2S0_TX_MCLK —** I^{2}S transmit master clock.
						I/O	**I2S1_RX_SCK —** Receive Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the *I^{2}S-bus specification*.
CLK3	P12	-	-	[4]	O; PU	O	**EMC_CLK2 —** SDRAM clock 2.
						O	**CLKOUT —** Clock output pin.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						O	**CGU_OUT1 —** CGU spare clock output 1.
						-	**R —** Function reserved.
						I/O	**I2S1_RX_SCK —** Receive Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the *I^{2}S-bus specification*.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA180	LQFP208		Reset state [1]	Type	Description
Debug pins							
DBGEN	L4	K4	41	[2]	I	I	JTAG interface control signal. Also used for boundary scan.
TCK/SWDCLK	J5	G5	38	[2]	I; F	I	Test Clock for JTAG interface (default) or Serial Wire (SW) clock.
$\overline{\mathrm{TRST}}$	M4	L4	42	[2]	I; PU	I	Test Reset for JTAG interface.
TMS/SWDIO	K6	K5	44	[2]	I; PU	I	Test Mode Select for JTAG interface (default) or SW debug data input/output.
TDO/SWO	K5	J5	46	[2]	O	O	Test Data Out for JTAG interface (default) or SW trace output.
TDI	J4	H4	35	[2]	I; PU	I	Test Data In for JTAG interface.
USB0 pins							
USB0_DP	F2	E2	26	[6]	-	I/O	USB0 bidirectional D+ line.
USB0_DM	G2	F2	28	[6]	-	I/O	USB0 bidirectional D– line.
USB0_VBUS	F1	E1	29	[6] [7]	-	I/O	VBUS pin (power on USB cable). This pin includes an internal pull-down resistor of 70 kΩ (typical) ± 30 kΩ.
USB0_ID	H2	G2	30	[8]	-	I	Indicates to the transceiver whether connected as an A-device (USB0_ID LOW) or B-device (USB0_ID HIGH). For use with OTG, this pin has an internal pull-up resistor.
USB0_RREF	H1	G1	32	[8]	-		12.0 kΩ (accuracy 1 %) on-board resistor to ground for current reference.
USB1 pins							
USB1_DP	F12	D11	129	[9]	-	I/O	USB1 bidirectional D+ line.
USB1_DM	G12	E11	130	[9]	-	I/O	USB1 bidirectional D– line.
I^{2}C-bus pins							
I2C0_SCL	L15	K13	132	[10]	I; F	I/O	I^{2}C clock input/output. Open-drain output (for I^{2}C-bus compliance).
I2C0_SDA	L16	K14	133	[10]	I; F	I/O	I^{2}C data input/output. Open-drain output (for I^{2}C-bus compliance).
Reset and wake-up pins							
$\overline{\mathrm{RESET}}$	D9	B7	185	[11]	I; IA	I	External reset input: A LOW on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0.
WAKEUP0	A9	A9	187	[11]	I; IA	I	External wake-up input; can raise an interrupt and can cause wake-up from any of the low power modes. A pulse with a duration of at least 45 ns wakes up the part. Input 0 of the event monitor.
WAKEUP1	A10	C8	-	[11]	I; IA	I	External wake-up input; can raise an interrupt and can cause wake-up from any of the low power modes. A pulse with a duration of at least 45 ns wakes up the part. Input 1 of the event monitor.
WAKEUP2	C9	E5	-	[11]	I; IA	I	External wake-up input; can raise an interrupt and can cause wake-up from any of the low power modes. A pulse with a duration of at least 45 ns wakes up the part. Input 2 of the event monitor.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA180	LQFP208		Reset state [1]	Type	Description
WAKEUP3	D8	-	-	[11]	I; IA	I	External wake-up input; can raise an interrupt and can cause wake-up from any of the low power modes. A pulse with a duration of at least 45 ns wakes up the part.
ADC pins							
ADC0_0/ ADC1_0/DAC	E3	B6	8	[8]	AI; IA	I	ADC input channel 0. Shared between 10-bit ADC0/1 and DAC.
ADC0_1/ ADC1_1	C3	C4	4	[8]	AI; IA	I	ADC input channel 1. Shared between 10-bit ADC0/1.
ADC0_2/ ADC1_2	A4	B3	206	[8]	AI; IA	I	ADC input channel 2. Shared between 10-bit ADC0/1.
ADC0_3/ ADC1_3	B5	B4	200	[8]	AI; IA	I	ADC input channel 3. Shared between 10-bit ADC0/1.
ADC0_4/ ADC1_4	C6	A5	199	[8]	AI; IA	I	ADC input channel 4. Shared between 10-bit ADC0/1.
ADC0_5/ ADC1_5	B3	C3	208	[8]	AI; IA	I	ADC input channel 5. Shared between 10-bit ADC0/1.
ADC0_6/ ADC1_6	A5	A4	204	[8]	AI; IA	I	ADC input channel 6. Shared between 10-bit ADC0/1.
ADC0_7/ ADC1_7	C5	B5	197	[8]	AI; IA	I	ADC input channel 7. Shared between 10-bit ADC0/1.
RTC pins							
RTC_ALARM	A11	A10	186	[11]	-	O	RTC controlled output.
RTCX1	A8	A8	182	[8]	-	I	Input to the RTC 32 kHz ultra-low power oscillator circuit.
RTCX2	B8	A7	183	[8]	-	O	Output from the RTC 32 kHz ultra-low power oscillator circuit.
$\overline{\text{SAMPLE}}$	B9	B8	-	[11]	O	O	Event monitor sample output.
Crystal oscillator pins							
XTAL1	D1	C1	18	[8]	-	I	Input to the oscillator circuit and internal clock generator circuits.
XTAL2	E1	D1	19	[8]	-	O	Output from the oscillator amplifier.
Power and ground pins							
USB0_VDDA 3V3_DRIVER	F3	E3	24		-	-	Separate analog 3.3 V power supply for driver.
USB0 _VDDA3V3	G3	F3	25		-	-	USB 3.3 V separate power supply voltage.
USB0_VSSA _TERM	H3	G3	27		-	-	Dedicated analog ground for clean reference for termination resistors.
USB0_VSSA _REF	G1	F1	31		-	-	Dedicated clean analog ground for generation of reference currents and voltages.
VDDA	B4	A6	198		-	-	Analog power supply and ADC reference voltage.
VBAT	B10	B9	184		-	-	RTC power supply: 3.3 V on this pin supplies power to the RTC.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA180	LQFP208		Reset state [1]	Type	Description
VDDREG	F10, F9, L8, L7	D8, E8	135, 188, 195, 82, 33			-	Main regulator power supply.
VPP	E8	-	-	[12]	-	-	OTP programming voltage.
VDDIO	D7, E12, F7, F8, G10, H10, J6, J7, K7, L9, L10, N7, N13	H5, H10, K8	6, 52, 57, 102, 110, 155, 160, 202	[12]	-	-	I/O power supply.
VSS	G9, H7, J10, J11, K8	F10, G10, D7, E6, E7, E9, K6, K9	-	[13]	-	-	Ground.
VSSIO	C4, D13, G6, G7, G8, H8, H9, J8, J9, K9, K10, M13, P7, P13	-	5, 56, 109, 157	[13]	-	-	Ground.
VSSA	B2	A3	196		-	-	Analog ground.

[1] N = neutral, input buffer disabled; no extra VDDIO current consumption if the input is driven midway between supplies; set the EZI bit in the SFS register to enable the input buffer; I = input, OL = output driving LOW; OH = output driving HIGH; AI/O = analog input/output; IA = inactive; PU = pull-up enabled (weak pull-up resistor pulls up pin to VDDIO; F = floating. Reset state reflects the pin state at reset without boot code operation.

[2] 5 V tolerant pad with 15 ns glitch filter (5 V tolerant if VDDIO present; if VDDIO not present, do not exceed 3.6 V); provides digital I/O functions with TTL levels and hysteresis; normal drive strength.

[3] 5 V tolerant pad with 15 ns glitch filter (5 V tolerant if VDDIO present; if VDDIO not present, do not exceed 3.6 V) providing digital I/O functions with TTL levels, and hysteresis; high drive strength.

[4] 5 V tolerant pad with 15 ns glitch filter (5 V tolerant if VDDIO present; if VDDIO not present, do not exceed 3.6 V) providing high-speed digital I/O functions with TTL levels and hysteresis.

[5] 5 V tolerant pad providing digital I/O functions (with TTL levels and hysteresis) and analog input or output (5 V tolerant if VDDIO present; if VDDIO not present, do not exceed 3.6 V). When configured as an ADC input or DAC output, the pin is not 5 V tolerant. For analog functionality, disable the digital section of the pad by setting the pin to an input function and by disabling the pull-up resistor through the corresponding SFSP register.

[6] 5 V tolerant transparent analog pad.

[7] For maximum load $C_L = 6.5\ \mu F$ and maximum resistance $R_{pd} = 80\ k\Omega$, the VBUS signal takes about 2 s to fall from VBUS = 5 V to VBUS = 0.2 V when it is no longer driven.

[8] Transparent analog pad. Not 5 V tolerant.

[9] Pad provides USB functions; It is designed in accordance with the USB specification, revision 2.0 (Full-speed and Low-speed mode only).

[10] Open-drain 5 V tolerant digital I/O pad, compatible with I^2C-bus Fast Mode Plus specification. This pad requires an external pull-up to provide output functionality. When power is switched off, this pin connected to the I^2C-bus is floating and does not disturb the I^2C lines.

[11] 5 V tolerant pad with 20 ns glitch filter; provides digital I/O functions with open-drain output with weak pull-up resistor and hysteresis.

[12] On the TFBGA180 and LQFP208 packages, VPP is internally connected to VDDIO.

[13] On the LQFP208 package, VSSIO and VSS are connected to a common ground plane.

7. Functional description

7.1 Architectural overview

The ARM Cortex-M3 includes three AHB-Lite buses: the system bus, the I-code bus, and the D-code bus. The I-code and D-code core buses allow for concurrent code and data accesses from different slave ports.

The LPC1857/53 use a multi-layer AHB matrix to connect the ARM Cortex-M3 buses and other bus masters to peripherals. Flexible connections allow different bus masters to access peripherals that are on different slave ports of the matrix simultaneously.

7.2 ARM Cortex-M3 processor

The ARM Cortex-M3 is a general purpose, 32-bit microprocessor, which offers high performance and low power consumption. The ARM Cortex-M3 offers many new features, including a Thumb-2 instruction set, low interrupt latency, hardware multiply and divide, interruptable/continuable multiple load and store instructions, automatic state save and restore for interrupts, tightly integrated interrupt controller with wake-up interrupt controller, and multiple core buses capable of simultaneous accesses.

Pipeline techniques are employed so that all parts of the processing and memory systems can operate continuously. Typically, while one instruction is being executed, its successor is being decoded, and a third instruction is being fetched from memory.

The ARM Cortex-M3 processor is described in detail in the Cortex-M3 Technical Reference Manual.

7.3 System Tick timer (SysTick)

The ARM Cortex-M3 includes a system tick timer (SYSTICK) that is intended to generate a dedicated SYSTICK exception at a 10 ms interval.

7.4 AHB multilayer matrix

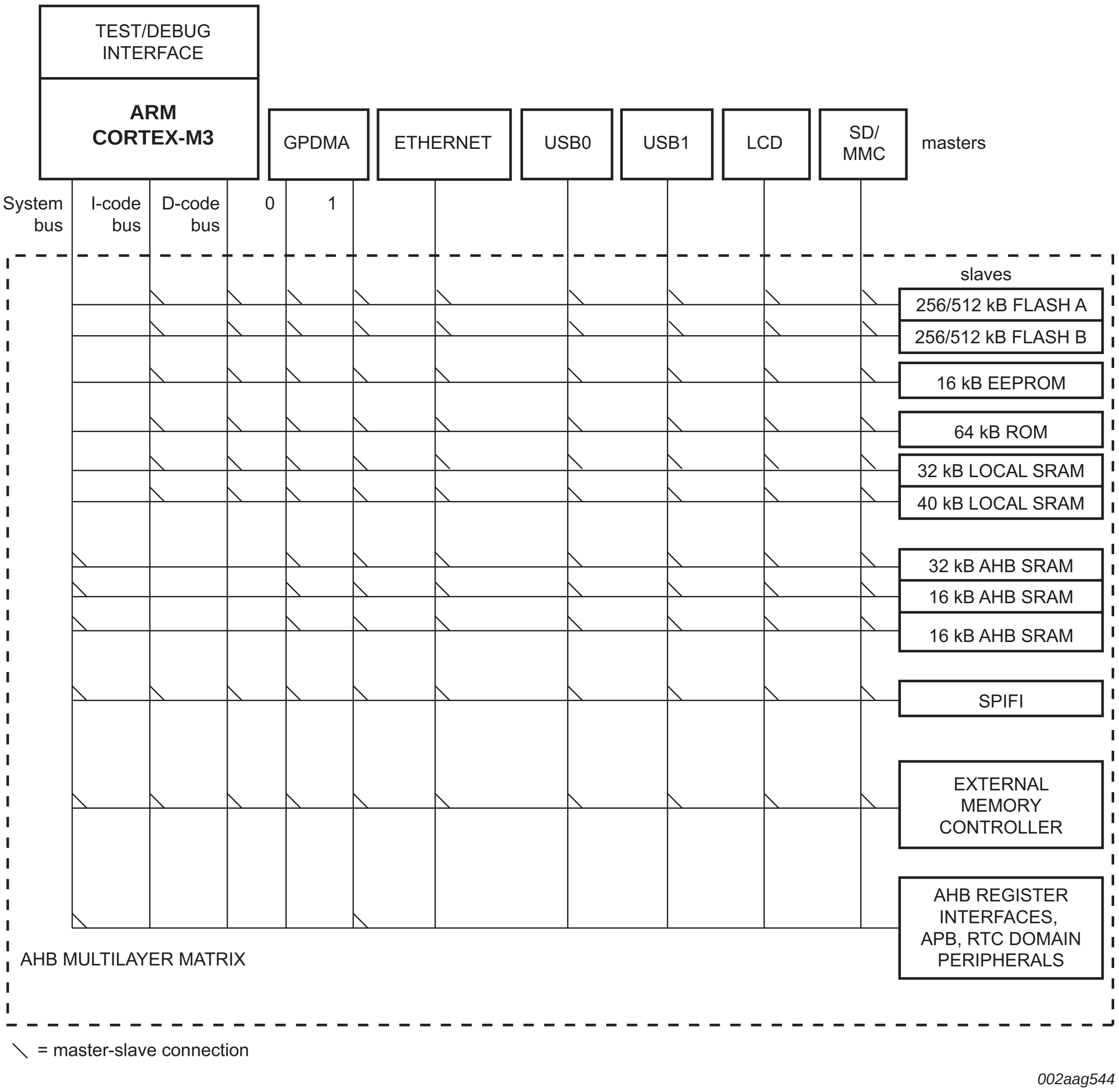


Fig 5. AHB multilayer matrix master and slave connections

7.5 Nested Vectored Interrupt Controller (NVIC)

The NVIC is part of the Cortex-M3. The tight coupling to the CPU allows for low interrupt latency and efficient processing of late arriving interrupts.

7.5.1 Features

- Controls system exceptions and peripheral interrupts.
- On the LPC1857/53, the NVIC supports 53 vectored interrupts.
- Eight programmable interrupt priority levels, with hardware priority level masking.
- Relocatable vector table.

- Non-Maskable Interrupt (NMI).
- Software interrupt generation.

7.5.2 Interrupt sources

Each peripheral device has one interrupt line connected to the NVIC but can have several interrupt flags. Individual interrupt flags can also represent more than one interrupt source.

7.6 Event router

The event router combines various internal signals, interrupts, and the external interrupt pins (WAKEUP[3:0]) to create an interrupt in the NVIC, if enabled. In addition, the event router creates a wake-up signal to the ARM core and the CCU for waking up from Sleep, Deep-sleep, Power-down, and Deep power-down modes. Individual events can be configured as edge or level sensitive and can be enabled or disabled in the event router. The event router can be battery powered.

The following events if enabled in the event router can create a wake-up signal from sleep, deep-sleep, power-down, and deep power-down modes and/or create an interrupt:

- External pins WAKEUP0/1/2/3 and $\overline{\text{RESET}}$
- Alarm timer, RTC (32 kHz oscillator running)

The following events if enabled in the event router can create a wake-up signal from sleep mode only and/or create an interrupt:

- WWDT, BOD interrupts
- C_CAN0/1 and QEI interrupts
- Ethernet, USB0, USB1 signals
- Selected outputs of combined timers (SCT and timer0/1/3)

Remark: Any interrupt can wake up the ARM Cortex-M3 from sleep mode if enabled in the NVIC.

7.7 Global Input Multiplexer Array (GIMA)

The GIMA allows to route signals to event-driven peripheral targets like the SCT, timers, event router, or the ADCs.

7.7.1 Features

- Single selection of a source.
- Signal inversion.
- Can capture a pulse if the input event source is faster than the target clock.
- Synchronization of input event and target clock.
- Single-cycle pulse generation for target.

7.8 On-chip static RAM

The LPC1857/53 support up to136 kB SRAM with separate bus master access for higher throughput and individual power control for low power operation.

7.9 On-chip flash memory

The LPC1857/53 contain up to 1 MB of dual-bank flash program memory. With dual-bank flash memory, the user code can write or erase one flash bank while reading the other flash bank without interruption. A two-port flash accelerator maximizes the flash performance.

In-System Programming (ISP) and In-Application Programming (IAP) routines for programming the flash memory are provided in the Boot ROM.

7.10 EEPROM

The LPC1857/53 contain up to 16 kB of on-chip byte-erasable and byte-programmable EEPROM memory.

The EEPROM memory is divided into 128 pages. The user can access pages 1 through 127. Page 128 is protected.

7.11 Boot ROM

The internal ROM memory is used to store the boot code of the LPC1857/53. After a reset, the ARM processor will start its code execution from this memory.

The boot ROM memory includes the following features:

- The ROM memory size is 64 kB.
- Supports booting from external static memory such as NOR flash, SPI flash, quad SPI flash, USB0, and USB1.
- Includes API for OTP programming.
- Includes a flexible USB device stack that supports Human Interface Device (HID), Mass Storage Class (MSC), and Device Firmware Upgrade (DFU) drivers.

AES capable parts also support:

- CMAC authentication on the boot image.
- Secure booting from an encrypted image. In development mode booting from a plain text image is possible. Development mode is terminated by programming the AES key.
- API for AES programming.

The default boot source is the flash memory. Several other boot modes are available if P2_7 is LOW on reset depending on the values of the OTP bits BOOT_SRC. If the OTP memory is not programmed or the BOOT_SRC bits are all zero, the states of the boot pins P2_9, P2_8, P1_2, and P1_1 determine the boot mode.

Table 4. Boot mode when OTP BOOT_SRC bits are programmed

Boot mode	BOOT_SRC bit 3	BOOT_SRC bit 2	BOOT_SRC bit 1	BOOT_SRC bit 0	Description
Pin state	0	0	0	0	The reset state of P1_1, P1_2, P2_8, and P2_9 pins determines the boot source. See Table 5.
USART0	0	0	0	1	Enter ISP mode using USART0 functions on pins P2_0 and P2_1.
SPIFI	0	0	1	0	Boot from Quad SPI flash connected to the SPIFI interface using pins P3_3 to P3_8.
EMC 8-bit	0	0	1	1	Boot from external static memory (such as NOR flash) using CS0 and an 8-bit data bus.
EMC 16-bit	0	1	0	0	Boot from external static memory (such as NOR flash) using CS0 and a 16-bit data bus.
EMC 32-bit	0	1	0	1	Boot from external static memory (such as NOR flash) using CS0 and a 32-bit data bus.
USB0	0	1	1	0	Boot from USB0.
USB1	0	1	1	1	Boot from USB1.
SPI (SSP)	1	0	0	0	Boot from SPI flash connected to the SSP0 interface on P3_3, P3_6, P3_7 and P3_8[1].
USART3	1	0	0	1	Enter ISP mode using USART3 functions on pins P2_3 and P2_4.

[1] The boot loader programs the appropriate pin function at reset to boot using either SSP0 or SPIFI.

Table 5. Boot mode when OPT BOOT_SRC bits are zero

Boot mode	Pins				Description
	P2_9	P2_8	P1_2	P1_1	
USART0	LOW	LOW	LOW	LOW	Enter ISP mode using USART0 pins P2_0 and P2_1.
SPIFI	LOW	LOW	LOW	HIGH	Boot from Quad SPI flash connected to the SPIFI interface on P3_3 to P3_8[1].
EMC 8-bit	LOW	LOW	HIGH	LOW	Boot from external static memory (such as NOR flash) using CS0 and an 8-bit data bus.
EMC 16-bit	LOW	LOW	HIGH	HIGH	Boot from external static memory (such as NOR flash) using CS0 and a 16-bit data bus.
EMC 32-bit	LOW	HIGH	LOW	LOW	Boot from external static memory (such as NOR flash) using CS0 and a 32-bit data bus.
USB0	LOW	HIGH	LOW	HIGH	Boot from USB0
USB1	LOW	HIGH	HIGH	LOW	Boot from USB1.
SPI (SSP)	LOW	HIGH	HIGH	HIGH	Boot from SPI flash connected to the SSP0 interface on P3_3, P3_6, P3_7 and P3_8[1].
USART3	HIGH	LOW	LOW	LOW	Enter ISP mode using USART3 pins P2_3 and P2_4.

[1] The boot loader programs the appropriate pin function at reset to boot using either SSP0 or SPIFI.

7.12 Memory mapping

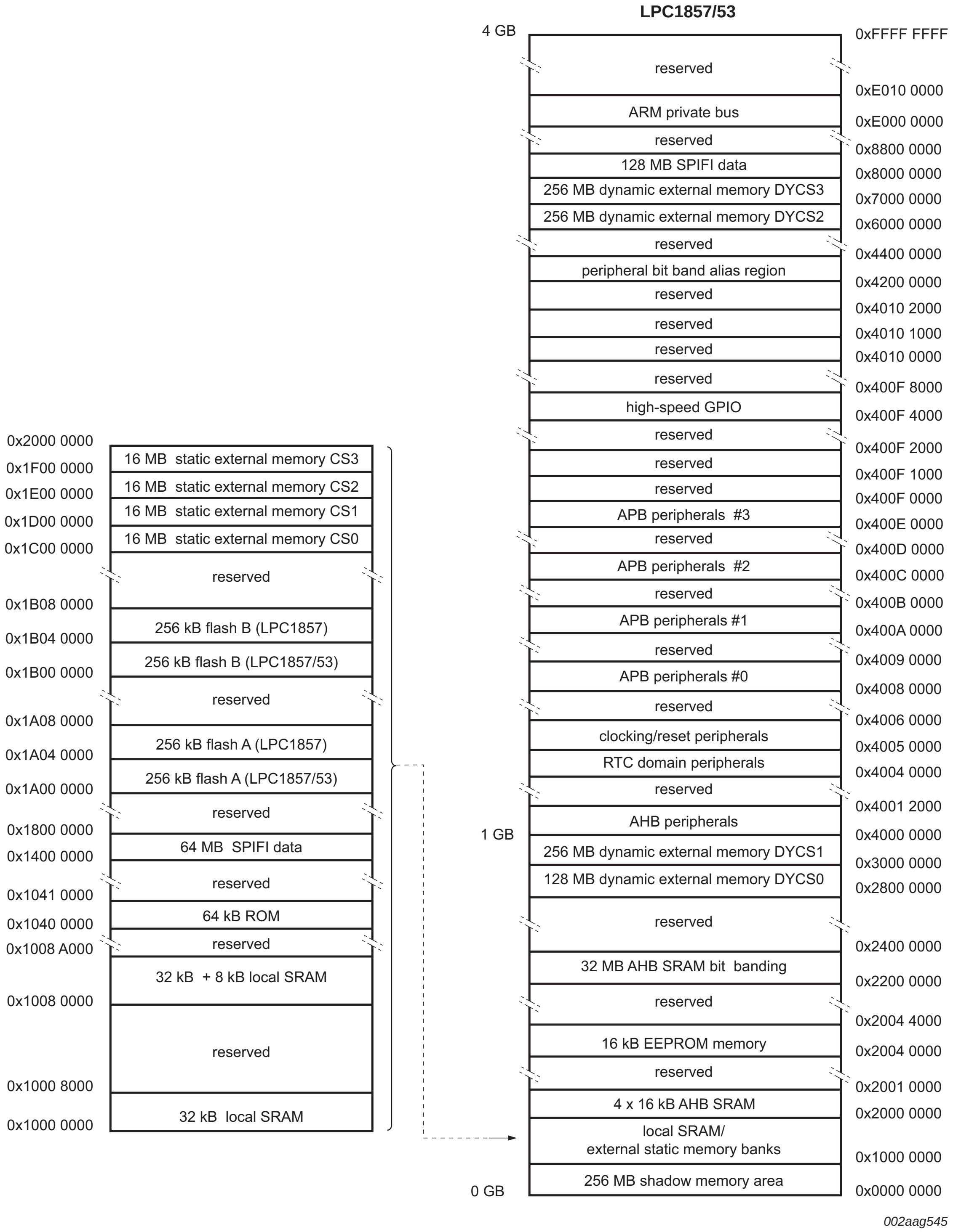


Fig 6. LPC1857/53 Memory mapping (overview)

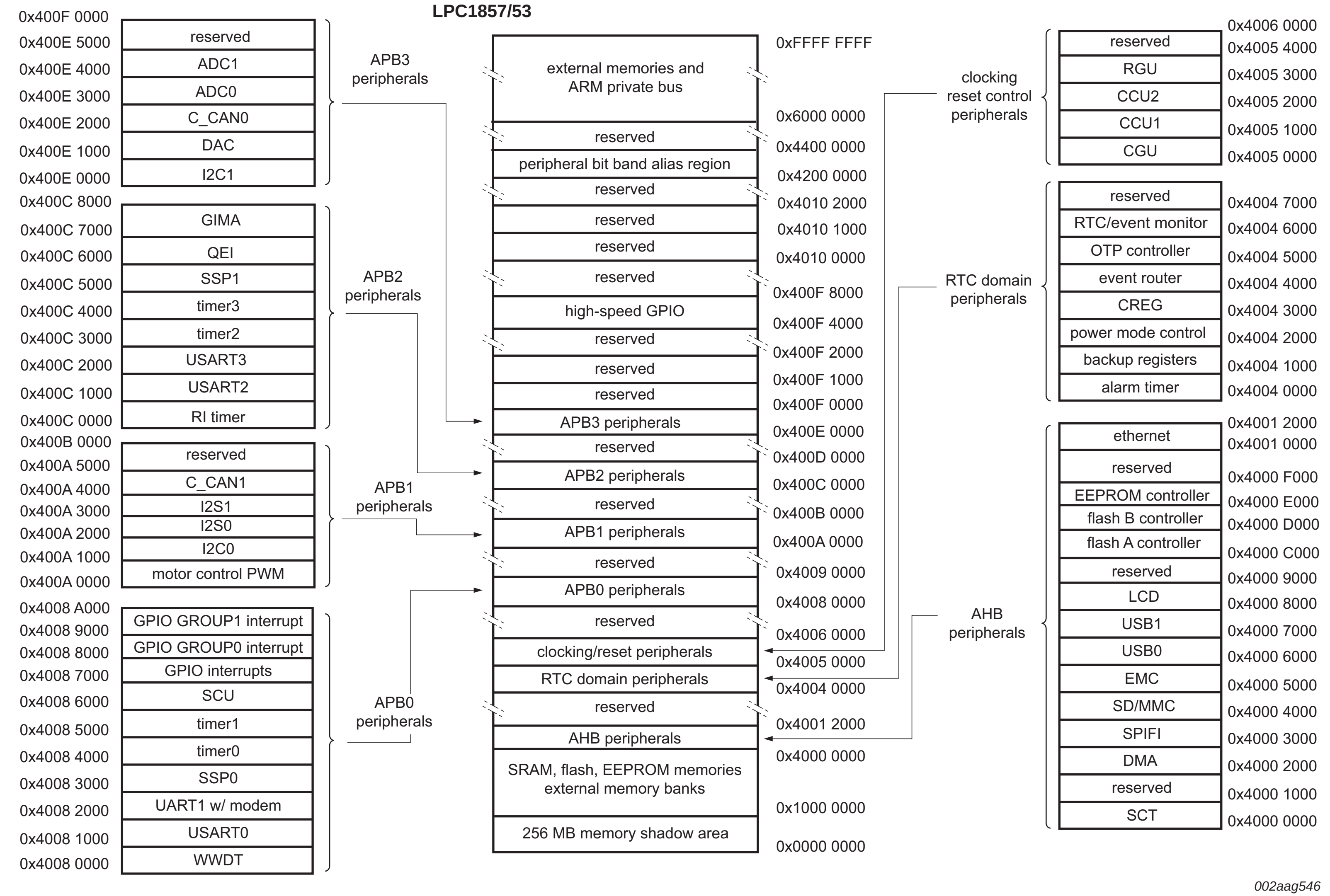


Fig 7. LPC1857/53 Memory mapping (peripherals)

7.13 Decryption features

7.13.1 AES decryption

The hardware AES decryption can decode data using the AES algorithm using a 128-bit key.

Remark: Once an AES key is programmed, no future factory testing can be performed on this device.

7.13.1.1 Features

- Decoding of external flash data connected to the quad SPI Flash Interface (SPIFI), EMC, or the USB0/1 interfaces.
- Secure storage of keys.
- Support for CMAC hash calculation to authenticate encrypted data.
- Data is processed in little endian mode. This means that the first byte read from flash is integrated into the AES codeword as least significant byte. The 16th byte read from flash is the most significant byte of the first AES codeword.
- AES engine performance of 1 byte/clock cycle.
- DMA transfers supported through the GPDMA.

7.13.2 One-Time Programmable (OTP) memory

The OTP provides 32 bit of memory for general-purpose use and two 128-bit non-volatile memory blocks to store AES keys or other customer data.

7.14 General Purpose I/O (GPIO)

The LPC1857/53 provides 8 GPIO ports with up to 31 GPIO pins each.

Device pins that are not connected to a specific peripheral function are controlled by the GPIO registers. Pins may be dynamically configured as inputs or outputs. Separate registers allow setting or clearing any number of outputs simultaneously. The value of the output register may be read back as well as the current state of the port pins.

All GPIO pins default to inputs with pull-up resistors enabled and input buffer disabled on reset. The input buffer must be turned on in the system control block SFS register before the GPIO input can be read.

7.14.1 Features

- Accelerated GPIO functions:
  - GPIO registers are located on the AHB so that the fastest possible I/O timing can be achieved.
  - Mask registers allow treating sets of port bits as a group, leaving other bits unchanged.
  - All GPIO registers are byte and half-word addressable.
  - Entire port value can be written in one instruction.
- Bit-level set and clear registers allow a single instruction set or clear of any number of bits in one port.

- Direction control of individual bits.
- Up to eight GPIO pins can be selected from all GPIO pins to create an edge- or level-sensitive GPIO interrupt request.
- Two GPIO group interrupts can be triggered by any pin or pins in each port.

7.15 AHB peripherals

7.15.1 State Configurable Timer (SCT) subsystem

The SCT allows a wide variety of timing, counting, output modulation, and input capture operations. The inputs and outputs of the SCT are shared with the capture and match inputs/outputs of the 32-bit general purpose counter/timers.

The SCT can be configured as two 16-bit counters or a unified 32-bit counter. In the two-counter case, in addition to the counter value the following operational elements are independent for each half:

- State variable
- Limit, halt, stop, and start conditions
- Values of Match/Capture registers, plus reload or capture control values

In the two-counter case, the following operational elements are global to the SCT, but the last three can use match conditions from either counter:

- Clock selection
- Inputs
- Events
- Outputs
- Interrupts

7.15.1.1 Features

- Two 16-bit counters or one 32-bit counter.
- Counters clocked by bus clock or selected input.
- Counters can be configured as up counters or up-down counters.
- State variable allows sequencing across multiple counter cycles.
- Event combines input or output condition and/or counter match in a specified state.
- Events control outputs and interrupts.
- Selected events can limit, halt, start, or stop a counter.
- Supports:
  - up to 8 inputs
  - up to 16 outputs
  - 16 match/capture registers
  - 16 events
  - 32 states

7.15.2 General-Purpose DMA (GPDMA)

The DMA controller allows peripheral-to memory, memory-to-peripheral, peripheral-to-peripheral, and memory-to-memory transactions. Each DMA stream provides unidirectional serial DMA transfers for a single source and destination. For example, a bidirectional port requires one stream for transmit and one for receives. The source and destination areas can each be either a memory region or a peripheral for master 1, but only memory for master 0.

7.15.2.1 Features

- Eight DMA channels. Each channel can support a unidirectional transfer.
- 16 DMA request lines.
- Single DMA and burst DMA request signals. Each peripheral connected to the DMA Controller can assert either a burst DMA request or a single DMA request. The DMA burst size is set by programming the DMA Controller.
- Memory-to-memory, memory-to-peripheral, peripheral-to-memory, and peripheral-to-peripheral transfers are supported.
- Scatter or gather DMA is supported through the use of linked lists. This means that the source and destination areas do not have to occupy contiguous areas of memory.
- Hardware DMA channel priority.
- AHB slave DMA programming interface. The DMA Controller is programmed by writing to the DMA control registers over the AHB slave interface.
- Two AHB bus masters for transferring data. These interfaces transfer data when a DMA request goes active. Master 1 can access memories and peripherals, master 0 can access memories only.
- 32-bit AHB master bus width.
- Incrementing or non-incrementing addressing for source and destination.
- Programmable DMA burst size. The DMA burst size can be programmed to more efficiently transfer data.
- Internal four-word FIFO per channel.
- Supports 8, 16, and 32-bit wide transactions.
- Big-endian and little-endian support. The DMA Controller defaults to little-endian mode on reset.
- An interrupt to the processor can be generated on a DMA completion or when a DMA error has occurred.
- Raw interrupt status. The DMA error and DMA count raw interrupt status can be read prior to masking.

7.15.3 SPI Flash Interface (SPIFI)

The SPI Flash Interface allows low-cost serial flash memories to be connected to the ARM Cortex-M3 processor with little performance penalty compared to parallel flash devices with higher pin count.

After a few commands configure the interface at startup, the entire flash content is accessible as normal memory using byte, halfword, and word accesses by the processor and/or DMA channels. Simple sequences of commands handle erasure and programming.

Many serial flash devices use a half-duplex command-driven SPI protocol for device setup and initialization and then move to a half-duplex, command-driven 4-bit protocol for normal operation. Different serial flash vendors and devices accept or require different commands and command formats. SPIFI provides sufficient flexibility to be compatible with common flash devices and includes extensions to help insure compatibility with future devices.

7.15.3.1 Features

- Interfaces to serial flash memory in the main memory map.
- Supports classic and 4-bit bidirectional serial protocols.
- Half-duplex protocol compatible with various vendors and devices.
- Quad SPI Flash Interface (SPIFI) with 1-, 2-, or 4-bit data at rates of up to 60 MB per second.
- Supports DMA access.

7.15.4 SD/MMC card interface

The SD/MMC card interface supports the following modes:

- Secure Digital memory (SD version 3.0)
- Secure Digital I/O (SDIO version 2.0)
- Consumer Electronics Advanced Transport Architecture (CE-ATA version 1.1)
- Multimedia Cards (MMC version 4.4)

7.15.5 External Memory Controller (EMC)

The LPC1857/53 EMC is a Memory Controller peripheral offering support for asynchronous static memory devices such as RAM, ROM, and NOR flash. In addition, it can be used as an interface with off-chip memory-mapped devices and peripherals.

7.15.5.1 Features

- Dynamic memory interface support including single data rate SDRAM.
- Asynchronous static memory device support including RAM, ROM, and NOR flash, with or without asynchronous page mode.
- Low transaction latency.
- Read and write buffers to reduce latency and to improve performance.
- 8/16/32 data and 24 address lines-wide static memory support.
- 16-bit and 32-bit wide chip select SDRAM memory support.
- Static memory features include:
  - Asynchronous page mode read
  - Programmable Wait States
  - Bus turnaround delay
  - Output enable and write enable delays
  - Extended wait
- Four chip selects for synchronous memory and four chip selects for static memory devices.

- Power-saving modes dynamically control CKE and CLKOUT to SDRAMs.
- Software-controlled dynamic memory self-refresh mode.
- Controller supports 2048 (A0 to A10), 4096 (A0 to A11), and 8192 (A0 to A12) row address synchronous memory parts. Those are typically 512 MB, 256 MB, and 128 MB parts.
- Separate reset domains allow auto-refresh through a chip reset if desired.

Note: Synchronous static memory devices (synchronous burst mode) are not supported.

7.15.6 High-speed USB Host/Device/OTG interface (USB0)

The USB OTG module allows the part to connect directly to a USB host such as a PC (in device mode) or to a USB device in host mode.

7.15.6.1 Features

- On-chip UTMI+ compliant high-speed transceiver (PHY).
- Complies with *Universal Serial Bus specification 2.0*.
- Complies with *USB On-The-Go supplement*.
- Complies with *Enhanced Host Controller Interface Specification*.
- Supports auto USB 2.0 mode discovery.
- Supports all high-speed USB-compliant peripherals.
- Supports all full-speed USB-compliant peripherals.
- Supports software Host Negotiation Protocol (HNP) and Session Request Protocol (SRP) for OTG peripherals.
- Supports interrupts.
- Supports Start Of Frame (SOF) frame length adjust.
- This module has its own, integrated DMA engine.

7.15.7 High-speed USB Host/Device interface with ULPI (USB1)

The USB1 interface can operate as a full-speed USB host/device interface or can connect to an external ULPI PHY for High-speed operation.

7.15.7.1 Features

- Complies with *Universal Serial Bus specification 2.0*.
- Complies with *Enhanced Host Controller Interface Specification*.
- Supports auto USB 2.0 mode discovery.
- Supports all high-speed USB-compliant peripherals if connected to external ULPI PHY.
- Supports all full-speed USB-compliant peripherals.
- Supports interrupts.
- Supports Start Of Frame (SOF) frame length adjust.
- This module has its own, integrated DMA engine.

7.15.8 LCD controller

The LCD controller provides all of the necessary control signals to interface directly to various color and monochrome LCD panels. Both STN (single and dual panel) and TFT panels can be operated. The display resolution is selectable and can be up to 1024 × 768 pixels. Several color modes are provided, up to a 24-bit true-color non-palettized mode. An on-chip 512 byte color palette allows reducing bus utilization (that is, memory size of the displayed data) while still supporting many colors.

The LCD interface includes its own DMA controller to allow it to operate independently of the CPU and other system functions. A built-in FIFO acts as a buffer for display data, providing flexibility for system timing. Hardware cursor support can further reduce the amount of CPU time required to operate the display.

7.15.8.1 Features

- AHB master interface to access frame buffer.
- Setup and control via a separate AHB slave interface.
- Dual 16-deep programmable 64-bit wide FIFOs for buffering incoming display data.
- Supports single and dual-panel monochrome Super Twisted Nematic (STN) displays with 4-bit or 8-bit interfaces.
- Supports single and dual-panel color STN displays.
- Supports Thin Film Transistor (TFT) color displays.
- Programmable display resolution including, but not limited to: 320 × 200, 320 × 240, 640 × 200, 640 × 240, 640 × 480, 800 × 600, and 1024 × 768.
- Hardware cursor support for single-panel displays.
- 15 gray-level monochrome, 3375 color STN, and 32 K color palettized TFT support.
- 1, 2, or 4 bits-per-pixel (bpp) palettized displays for monochrome STN.
- 1, 2, 4, or 8 bpp palettized color displays for color STN and TFT.
- 16 bpp true-color non-palettized for color STN and TFT.
- 24 bpp true-color non-palettized for color TFT.
- Programmable timing for different display panels.
- 256 entry, 16-bit palette RAM, arranged as a 128 × 32-bit RAM.
- Frame, line, and pixel clock signals.
- AC bias signal for STN, data enable signal for TFT panels.
- Supports little and big-endian, and Windows CE data formats.
- LCD panel clock can be generated from the peripheral clock, or from a clock input pin.

7.15.9 Ethernet

7.15.9.1 Features

- 10/100 Mbit/s
- DMA support
- Power management remote wake-up frame and magic packet detection
- Supports both full-duplex and half-duplex operation

  - Supports CSMA/CD Protocol for half-duplex operation.
  - Supports IEEE 802.3x flow control for full-duplex operation.
  - Optional forwarding of received pause control frames to the user application in full-duplex operation.
  - Back-pressure support for half-duplex operation.
  - Automatic transmission of zero-quanta pause frame on deassertion of flow control input in full-duplex operation.
- Support for IEEE 1588 time stamping and IEEE 1588 advanced time stamping (IEEE 1588-2008 v2).

7.16 Digital serial peripherals

7.16.1 UART

Remark: The LPC1857/53 contain one UART with standard transmit and receive data lines.

UART1 also provides a full modem control handshake interface and support for RS-485/9-bit mode allowing both software address detection and automatic address detection using 9-bit mode.

UART1 includes a fractional baud rate generator. Standard baud rates such as 115200 Bd can be achieved with any crystal frequency above 2 MHz.

7.16.1.1 Features

- Maximum UART data bit rate of 8 MBit/s.
- 16 B Receive and Transmit FIFOs.
- Register locations conform to 16C550 industry standard.
- Receiver FIFO trigger points at 1 B, 4 B, 8 B, and 14 B.
- Built-in fractional baud rate generator covering wide range of baud rates without a need for external crystals of particular values.
- Auto baud capabilities and FIFO control mechanism that enables software flow control implementation.
- Equipped with standard modem interface signals. This module also provides full support for hardware flow control (auto-CTS/RTS).
- Support for RS-485/9-bit/EIA-485 mode (UART1).
- DMA support.

7.16.2 USART

Remark: The LPC1857/53 contain three USARTs. In addition to standard transmit and receive data lines, the USARTs support a synchronous mode and a smart card mode.

The USARTs include a fractional baud rate generator. Standard baud rates such as 115200 Bd can be achieved with any crystal frequency above 2 MHz.

7.16.2.1 Features

- Maximum UART data bit rate of 8 MBit/s.

- 16 B Receive and Transmit FIFOs.
- Register locations conform to 16C550 industry standard.
- Receiver FIFO trigger points at 1 B, 4 B, 8 B, and 14 B.
- Built-in fractional baud rate generator covering wide range of baud rates without a need for external crystals of particular values.
- Auto baud capabilities and FIFO control mechanism that enables software flow control implementation.
- Support for RS-485/9-bit/EIA-485 mode.
- USART3 includes an IrDA mode to support infrared communication.
- All USARTs have DMA support.
- Support for synchronous mode at a data bit rate of up to 8 Mbit/s.
- Smart card mode conforming to ISO7816 specification

7.16.3 SSP serial I/O controller

Remark: The LPC1857/53 contain two SSP controllers.

The SSP controller can operate on a SPI, 4-wire SSI, or Microwire bus. It can interact with multiple masters and slaves on the bus. Only a single master and a single slave can communicate on the bus during a given data transfer. The SSP supports full duplex transfers, with frames of 4 bit to 16 bit of data flowing from the master to the slave and from the slave to the master. In practice, often only one of these data flows carries meaningful data.

7.16.3.1 Features

- Maximum SSP speed of <tbd> Mbit/s (master) or <tbd> Mbit/s (slave)
- Compatible with Motorola SPI, 4-wire Texas Instruments SSI, and National Semiconductor Microwire buses
- Synchronous serial communication
- Master or slave operation
- Eight-frame FIFOs for both transmit and receive
- 4-bit to 16-bit frame
- Connected to the GPDMA

7.16.4 I^{2}C-bus interface

Remark: The LPC1857/53 each contain two I^{2}C-bus interfaces.

The I^{2}C-bus is bidirectional for inter-IC control using only two wires: a Serial Clock line (SCL) and a Serial Data line (SDA). Each device is recognized by a unique address and can operate as either a receiver-only device (for example, an LCD driver) or a transmitter with the capability to both receive and send information (such as memory). Transmitters and/or receivers can operate in either master or slave mode, depending on whether the chip has to initiate a data transfer or is only addressed. The I^{2}C-bus interface is a multi-master bus and can be controlled by more than one bus master connected to it.

7.16.4.1 Features

- I^2C0 is a standard I^2C-bus compliant bus interface with open-drain pins. I^2C0 also supports Fast mode plus with bit rates up to 1 Mbit/s.
- I^2C1 uses standard I/O pins with bit rates of up to 400 kbit/s (Fast I^2C-bus).
- Easy to configure as master, slave, or master/slave.
- Programmable clocks allow versatile rate control.
- Bidirectional data transfer between masters and slaves.
- Multi-master bus (no central master).
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus.
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus.
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer.
- The I^2C-bus can be used for test and diagnostic purposes.
- All I^2C-bus controllers support multiple address recognition and a bus monitor mode.

7.16.5 I^2S interface

Remark: The LPC1857/53 contain two I^2S interfaces.

The I^2S-bus provides a standard communication interface for digital audio applications.

The *I^2S-bus specification* defines a 3-wire serial bus using one data line, one clock line, and one word select signal. The basic I^2S-bus connection has one master, which is always the master, and one slave. The I^2S-bus interface provides a separate transmit and receive channel, each of which can operate as either a master or a slave.

7.16.5.1 Features

- The interface has separate input/output channels each of which can operate in master or slave mode.
- Capable of handling 8-bit, 16-bit, and 32-bit word sizes.
- Mono and stereo audio data supported.
- The sampling frequency can range from 16 kHz to 192 kHz (16, 22.05, 32, 44.1, 48, 96, 192) kHz.
- Support for an audio master clock.
- Configurable word select period in master mode (separately for I^2S-bus input and output).
- Two 8-word FIFO data buffers are provided, one for transmit and one for receive.
- Generates interrupt requests when buffer levels cross a programmable boundary.
- Two DMA requests, controlled by programmable buffer levels. The DMA requests are connected to the GPDMA block.
- Controls include reset, stop and mute options separately for I^2S-bus input and I^2S-bus output.

7.16.6 C_CAN

Remark: The LPC1857/53 contain two C_CAN controllers.

Controller Area Network (CAN) is the definition of a high performance communication protocol for serial data communication. The C_CAN controller is designed to provide a full implementation of the CAN protocol according to the CAN Specification Version 2.0B. The C_CAN controller allows to build powerful local networks with low-cost multiplex wiring by supporting distributed real-time control with a high level of reliability.

7.16.6.1 Features

- Conforms to protocol version 2.0 parts A and B.
- Supports bit rate of up to 1 Mbit/s.
- Supports 32 Message Objects.
- Each Message Object has its own identifier mask.
- Provides programmable FIFO mode (concatenation of Message Objects).
- Provides maskable interrupts.
- Supports Disabled Automatic Retransmission (DAR) mode for time-triggered CAN applications.
- Provides programmable loop-back mode for self-test operation.

7.17 Counter/timers and motor control

7.17.1 General purpose 32-bit timers/external event counter

Remark: The LPC1857/53 include four 32-bit timer/counters.

The timer/counter is designed to count cycles of the system derived clock or an externally supplied clock. It can optionally generate interrupts, generate timed DMA requests, or perform other actions at specified timer values, based on four match registers. Each timer/counter also includes two capture inputs to trap the timer value when an input signal transitions, optionally generating an interrupt.

7.17.1.1 Features

- A 32-bit timer/counter with a programmable 32-bit prescaler.
- Counter or timer operation.
- Two 32-bit capture channels per timer, that can take a snapshot of the timer value when an input signal transitions. A capture event can also generate an interrupt.
- Four 32-bit match registers that allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
- Up to four external outputs corresponding to match registers, with the following capabilities:
  - Set LOW on match.
  - Set HIGH on match.

  - Toggle on match.
  - Do nothing on match.
- Up to two match registers can be used to generate timed DMA requests.

7.17.2 Motor control PWM

The motor control PWM is a specialized PWM supporting 3-phase motors and other combinations. Feedback inputs are provided to automatically sense rotor position and use that information to ramp speed up or down. An abort input causes the PWM to release all motor drive outputs immediately . At the same time, the motor control PWM is highly configurable for other generalized timing, counting, capture, and compare applications.

7.17.3 Quadrature Encoder Interface (QEI)

A quadrature encoder, also known as a 2-channel incremental encoder, converts angular displacement into two pulse signals. By monitoring both the number of pulses and the relative phase of the two signals, the user code can track the position, direction of rotation, and velocity. In addition, a third channel, or index signal, can be used to reset the position counter. The quadrature encoder interface decodes the digital pulses from a quadrature encoder wheel to integrate position over time and determine direction of rotation. In addition, the QEI can capture the velocity of the encoder wheel.

7.17.3.1 Features

- Tracks encoder position.
- Increments/decrements depending on direction.
- Programmable for 2× or 4× position counting.
- Velocity capture using built-in timer.
- Velocity compare function with “less than” interrupt.
- Uses 32-bit registers for position and velocity.
- Three position compare registers with interrupts.
- Index counter for revolution counting.
- Index compare register with interrupts.
- Can combine index and position interrupts to produce an interrupt for whole and partial revolution displacement.
- Digital filter with programmable delays for encoder input signals.
- Can accept decoded signal inputs (clk and direction).

7.17.4 Repetitive Interrupt (RI) timer

The repetitive interrupt timer provides a free-running 32-bit counter which is compared to a selectable value, generating an interrupt when a match occurs. Any bits of the timer compare function can be masked such that they do not contribute to the match detection. The repetitive interrupt timer can be used to create an interrupt that repeats at predetermined intervals.

7.17.4.1 Features

- 32-bit counter. Counter can be free-running or be reset by a generated interrupt.
- 32-bit compare value.

- 32-bit compare mask. An interrupt is generated when the counter value equals the compare value, after masking. This mechanism allows for combinations not possible with a simple compare.

7.17.5 Windowed WatchDog Timer (WWDT)

The purpose of the watchdog is to reset the controller if software fails to periodically service it within a programmable time window.

7.17.5.1 Features

- Internally resets chip if not periodically reloaded during the programmable time-out period.
- Optional windowed operation requires reload to occur between a minimum and maximum time period, both programmable.
- Optional warning interrupt can be generated at a programmable time prior to watchdog time-out.
- Enabled by software but requires a hardware reset or a watchdog reset/interrupt to be disabled.
- Incorrect feed sequence causes reset or interrupt if enabled.
- Flag to indicate watchdog reset.
- Programmable 24-bit timer with internal prescaler.
- Selectable time period from ($T_{cy(WDCLK)} \times 256 \times 4$) to ($T_{cy(WDCLK)} \times 2^{24} \times 4$) in multiples of $T_{cy(WDCLK)} \times 4$.
- The Watchdog Clock (WDCLK) uses the IRC as the clock source.

7.18 Analog peripherals

7.18.1 Analog-to-Digital Converter

Remark: The LPC1857/53 contain two 10-bit ADCs.

7.18.1.1 Features

- 10-bit successive approximation analog to digital converter.
- Input multiplexing among 8 pins.
- Power-down mode.
- Measurement range 0 to VDDA.
- Sampling frequency up to 400 kSamples/s.
- Burst conversion mode for single or multiple inputs.
- Optional conversion on transition on ADCTRIG0 or ADCTRIG1 pins, combined timer outputs 8 or 15, or the PWM output MCOA2.
- Individual result registers for each A/D channel to reduce interrupt overhead.
- DMA support.

7.18.2 Digital-to-Analog Converter (DAC)

7.18.2.1 Features

- 10-bit resolution
- Monotonic by design (resistor string architecture)
- Controllable conversion speed
- Low power consumption

7.19 Peripherals in the RTC power domain

7.19.1 RTC

The Real Time Clock (RTC) is a set of counters for measuring time when system power is on, and optionally when it is off. It uses little power when the CPU does not access its registers, especially in the reduced power modes. A separate 32 kHz oscillator clocks the RTC. The oscillator produces a 1 Hz internal time reference and is powered by its own power supply pin, VBAT.

7.19.1.1 Features

- Measures the passage of time to maintain a calendar and clock. Provides seconds, minutes, hours, day of month, month, year, day of week, and day of year.
- Ultra-low power design to support battery powered systems. Uses power from the CPU power supply when it is present.
- Dedicated battery power supply pin.
- RTC power supply is isolated from the rest of the chip.
- Calibration counter allows adjustment to better than ±1 sec/day with 1 sec resolution.
- Periodic interrupts can be generated from increments of any field of the time registers.
- Alarm interrupt can be generated for a specific date/time.

7.19.2 Event monitor/recorder

The event monitor/recorder allows recording and creating a time stamp of events related to the WAKEUP pins. Sensors report changes to the state of the WAKEUP pins, and the event monitor/recorder stores records of such events. The event recorder can be powered by the backup battery.

The event monitor/recorder can monitor the integrity of the device and record any tampering events.

7.19.2.1 Features

- Supports three digital event inputs in the VBAT power domain.
- An event is defined as a level change at the digital event inputs.
- For each event channel, two timestamps mark the first and the last occurrence of an event. Each channel also has a dedicated counter tracking the total number of events. Timestamp values are taken from the RTC.
- Runs in VBAT power domain, independent of system power supply. The event/recorder/monitor can therefore operate in Deep power-down mode.

- Low power consumption.
- Interrupt available if system is running.
- A qualified event can be used as a wake-up trigger.
- State of event interrupts accessible by software through GPIO.

7.19.3 Alarm timer

The alarm timer is a 16-bit timer and counts down at 1 kHz from a preset value generating alarms in intervals of up to 1 min. The counter triggers a status bit when it reaches 0x00 and asserts an interrupt, if enabled.

The alarm timer is part of the RTC power domain and can be battery powered.

7.20 System control

7.20.1 Configuration registers (CREG)

The following settings are controlled in the configuration register block:

- BOD trip settings
- Oscillator output
- DMA-to-peripheral muxing
- Ethernet mode
- Memory mapping
- Timer/USART inputs
- Enabling the USB controllers

In addition, the CREG block contains the part identification and part configuration information.

7.20.2 System Control Unit (SCU)

The system control unit determines the function and electrical mode of the digital pins. By default function 0 is selected for all pins with pull-up enabled. For pins that support a digital and analog function, the ADC function select registers in the SCU enable the analog function.

A separate set of analog I/Os for the ADCs and the DAC as well as most USB pins are located on separate pads and are not controlled through the SCU.

In addition, the clock delay register for the SDRAM EMC_CLK pins and the registers that select the pin interrupts are located in the SCU.

7.20.3 Clock Generation Unit (CGU)

The Clock Generator Unit (CGU) generates several base clocks. The base clocks can be unrelated in frequency and phase and can have different clock sources within the CGU. One CGU base clock is routed to the CLKOUT pins. The base clock that generates the CPU clock is referred to as CCLK.

Multiple branch clocks are derived from each base clock. The branch clocks offer flexible control for power-management purposes. All branch clocks are outputs of one of two Clock Control Units (CCUs) and can be controlled independently. Branch clocks derived from the same base clock are synchronous in frequency and phase.

7.20.4 Internal RC oscillator (IRC)

The IRC is used as the clock source for the WWDT and/or as the clock that drives the PLLs and the CPU. The nominal IRC frequency is 12 MHz. The IRC is trimmed to 1 % accuracy over the entire voltage and temperature range.

Upon power-up or any chip reset, the LPC1857/53 use the IRC as the clock source. The boot loader then configures the PLL1 to provide a 96 MHz clock for the core and the PLL0USB or PLL0AUDIO as needed if an external boot source is selected.

7.20.5 PLL0USB (for USB0)

PLL0 is a dedicated PLL for the USB0 High-speed controller.

PLL0 accepts an input clock frequency from an external oscillator in the range of 14 kHz to 25 MHz. The input frequency is multiplied up to a high frequency with a Current Controlled Oscillator (CCO). The CCO operates in the range of 4.3 MHz to 550 MHz.

7.20.6 PLL0AUDIO (for audio)

The audio PLL PLL0AUDIO is a general-purpose PLL with a small step size. This PLL accepts an input clock frequency derived from an external oscillator or internal IRC. The input frequency is multiplied up to a high frequency with a Current Controlled Oscillator (CCO). A sigma-delta converter modulates the PLL divider ratios to obtain the desired output frequency. The output frequency can be set as a multiple of the sampling frequency f_S to $32 \times f_S$, $64 \times f_S$, $128 \times f_S$, $256 \times f_S$, $384 \times f_S$, $512 \times f_S$ and the sampling frequency f_S can range from 16 kHz to 192 kHz (16, 22.05, 32, 44.1, 48, 96,192) kHz. Many other frequencies are possible as well using the integrated fractional divider.

7.20.7 System PLL1

The PLL1 accepts an input clock frequency from an external oscillator in the range of 10 MHz to 25 MHz. The input frequency is multiplied up to a high frequency with a Current Controlled Oscillator (CCO). The multiplier can be an integer value from 1 to 32. The CCO operates in the range of 156 MHz to 320 MHz. This range is possible through an additional divider in the loop to keep the CCO within its frequency range while the PLL is providing the desired output frequency. The output divider can be set to divide by 2, 4, 8, or 16 to produce the output clock. Since the minimum output divider value is 2, it is insured that the PLL output has a 50 % duty cycle. The PLL is turned off and bypassed following a chip reset. After reset, software can enable the PLL. The program must configure and activate the PLL, wait for the PLL to lock, and then connect to the PLL as a clock source. The PLL settling time is 100 μs.

7.20.8 Reset Generation Unit (RGU)

The RGU allows generation of independent reset signals for individual blocks and peripherals.

7.20.9 Power control

The LPC1857/53 feature several independent power domains to control power to the core and the peripherals (see Figure 8). The RTC and its associated peripherals (the alarm timer, the CREG block, the OTP controller, the back-up registers, and the event router) are located in the RTC power-domain. The main regulator or a battery supply can power the RTC. A power selector switch ensures that the RTC block is always powered on.

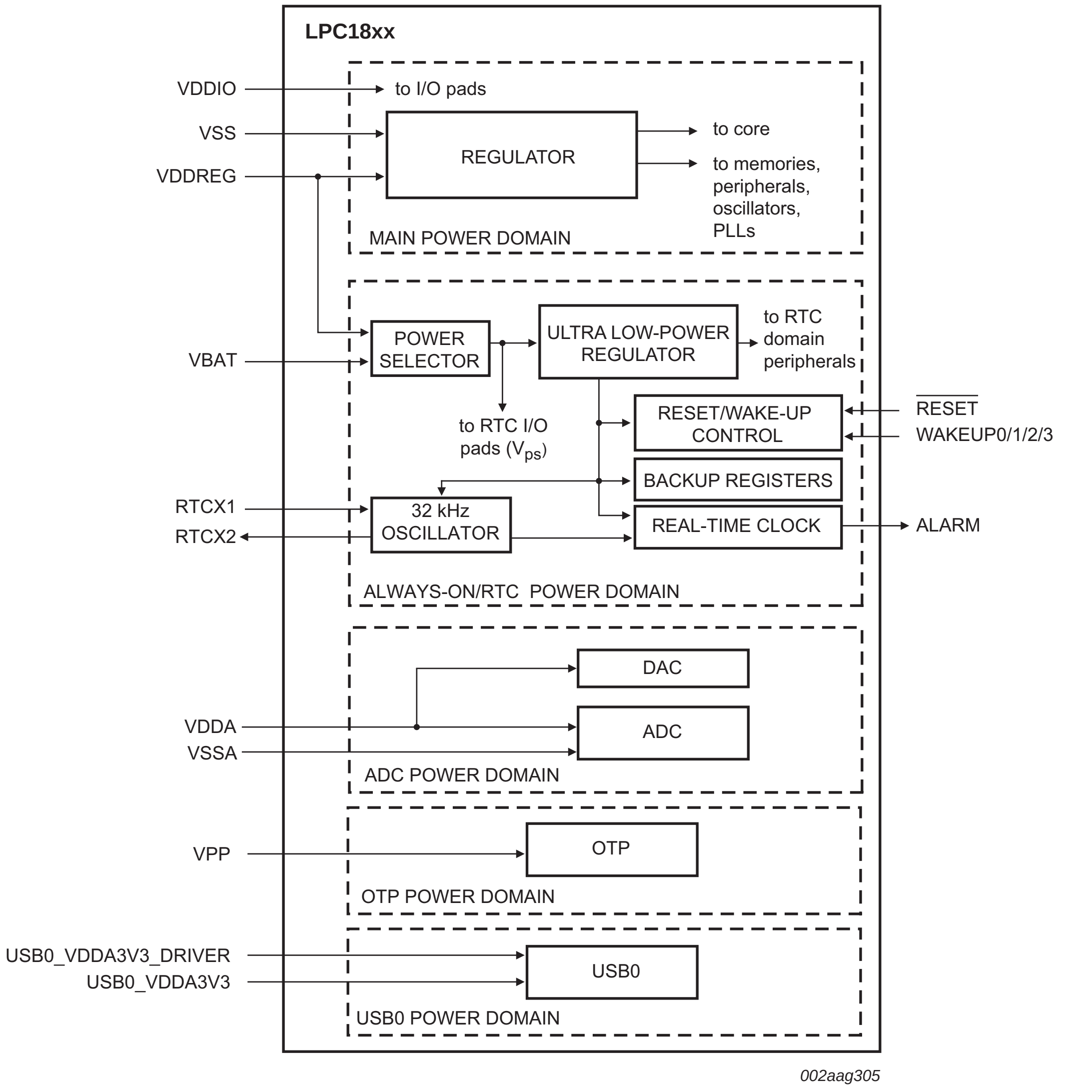


Fig 8. LPC1857/53 Power domains

The LPC1857/53 support four reduced power modes: Sleep, Deep-sleep, Power-down, and Deep power-down.

The LPC1857/53 can wake up from Deep-sleep, Power-down, and Deep power-down modes via the WAKEUP[3:0] pins and interrupts generated by battery powered blocks in the RTC power domain.

7.20.10 Code security (Code Read Protection - CRP)

CRP enables different levels of security so that access to the on-chip flash and use of the JTAG and ISP can be restricted. CRP is invoked by programming a specific pattern into a dedicated flash location. IAP commands are not affected by CRP.

There are three levels of the Code Read Protection:

- In level CRP1, access to the chip via the JTAG is disabled. Partial flash updates are allowed (excluding flash sector 0) using a limited set of the ISP commands. This level is useful when CRP is required and flash field updates are needed. CRP1 does prevent the user code from erasing all sectors.
- In level CRP2, access to the chip via the JTAG is disabled. Only a full flash erase and update using a reduced set of the ISP commands is allowed.
- In level CRP3, any access to the chip via the JTAG pins or the ISP is disabled. This mode also disables the ISP override using P2_7 pin. If necessary, the application code must provide a flash update mechanism using the IAP calls or using the reinvoke ISP command to enable flash update via USART0.

CAUTION

⚠

If level three Code Read Protection (CRP3) is selected, no future factory testing can be performed on the device.

7.21 Emulation and debugging

Debug and trace functions are integrated into the ARM Cortex-M3. Serial wire debug and trace functions are supported in addition to a standard JTAG debug and parallel trace functions. The ARM Cortex-M3 is configured to support up to eight breakpoints and four watch points.

8. Limiting values

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{DD(REG)(3V3)}$	regulator supply voltage (3.3 V)	on pin VDDREG		2.2	3.6	V
$V_{DD(IO)}$	input/output supply voltage	on pin VDDIO		2.2	3.6	V
$V_{DDA(3V3)}$	analog supply voltage (3.3 V)	on pin VDDA		2.2	3.6	V
V_{BAT}	battery supply voltage	on pin VBAT		2.2	3.6	V
$V_{prog(pf)}$	polyfuse programming voltage	on pin VPP		2.7	3.6	V
V_I	input voltage	when $V_{DD(IO)} \geq 2.2$ V 5 V tolerant digital I/O pins	[2]	–0.5	5.5	V
		ADC/DAC pins and digital I/O pins configured for an analog function		–0.5	$V_{DDA(3V3)}$	V
		USB0 pins USB0_DP; USB0_DM;USB0_VBUS		0	5.2	V
		USB0 pins USB0_ID; USB0_RREF		0	3.6	V
		USB1 pins USB1_DP and USB1_DM		0	5.2	V
I_{DD}	supply current	per supply pin	[3]	-	100	mA
I_{SS}	ground current	per ground pin	[3]	-	100	mA
I_{latch}	I/O latch-up current	$-(0.5V_{DD(IO)}) < V_I < (1.5V_{DD(IO)})$; $T_j < 125$ °C		-	100	mA
T_{stg}	storage temperature		[4]	–65	+150	°C
$P_{tot(pack)}$	total power dissipation (per package)	based on package heat transfer, not device power consumption		-	1.5	W
V_{ESD}	electrostatic discharge voltage	human body model; all pins	[5]	–2000	+2000	V

[1] The following applies to the limiting values:

a) This product includes circuitry designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.

b) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

[2] Including voltage on outputs in 3-state mode.

[3] The peak current is limited to 25 times the corresponding maximum current.

[4] Dependent on package type.

[5] Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

9. Thermal characteristics

The average chip junction temperature, T_j (°C), can be calculated using the following equation:

$$T_j = T_{amb} + (P_D \times R_{th(j-a)}) \qquad (1)$$

- T_{amb} = ambient temperature (°C),
- $R_{th(j-a)}$ = the package junction-to-ambient thermal resistance (°C/W)
- P_D = sum of internal and I/O power dissipation

The internal power dissipation is the product of I_{DD} and V_{DD}. The I/O power dissipation of the I/O pins is often small and many times can be negligible. However it can be significant in some applications.

Table 7. Thermal characteristics

V_{DD} = 2.2 V to 3.6 V; T_{amb} = −40 °C to +85 °C unless otherwise specified;

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{j(max)}$	maximum junction temperature		-	-	<tbd>	°C

10. Static characteristics

Table 8. Static characteristics

T_{amb} = –40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
Supply pins							
$V_{DD(IO)}$	input/output supply voltage			2.2	-	3.6	V
$V_{DD(REG)(3V3)}$	regulator supply voltage (3.3 V)		[2]	2.2	-	3.6	V
$V_{DDA(3V3)}$	analog supply voltage (3.3 V)	on pin VDDA		2.2	-	3.6	V
V_{BAT}	battery supply voltage			2.2	-	3.6	V
$V_{prog(pf)}$	polyfuse programming voltage	on pin VPP (for OTP)	[3]	2.7	-	3.6	V
$V_{DD(3V3)}$	supply voltage (3.3 V)	on pin V_{DD};		2.2	-	3.6	V
$I_{prog(pf)}$	polyfuse programming current	on pin VPP; OTP programming time ≤ 1.6 ms		-	-	30	mA
$I_{DD(REG)(3V3)}$	regulator supply current (3.3 V)	Regulator supply <tbd> mode; code `while(1){}` executed from flash; all peripherals disabled					
		CCLK = 12 MHz; PLL1 disabled	[4][5]	-	<tbd>	-	mA
		CCLK = 12 MHz; PLL1 enabled	[4][6]	-	<tbd>	-	mA
		CCLK = 120 MHz	[4][6]	-	<tbd>	-	mA
		CCLK = 156 MHz	[4][6]	-	<tbd>	-	mA
$I_{DD(REG)(3V3)}$	regulator supply current (3.3 V)	Regulator supply <tbd> mode; after WFE/WFI instruction executed from RAM; all peripherals disabled					
		sleep mode	[4][5]	-	<tbd>	-	mA
		deep-sleep mode	[4]	-	<tbd>	-	µA
		power-down mode	[4]	-	<tbd>	-	µA
		deep power-down mode	[4]	-	<tbd>	-	µA
I_{BAT}	battery supply current	deep-sleep mode	[4][7]	-	<tbd>		µA
		power-down mode	[4][7]	-	<tbd>	-	µA
		deep power-down mode	[4][7]	-	<tbd>	-	µA
$I_{DD(IO)}$	I/O supply current	deep sleep mode		-	<tbd>	-	µA
		power-down mode		-	<tbd>	-	µA
		deep power-down mode		-	<tbd>	-	µA

Table 8. Static characteristics *…continued*

T_{amb} = –40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
$I_{DD(ADC)}$	ADC supply current	deep sleep mode	[9]	-	0.4	-	µA
		power-down mode	[9]	-	0.4	-	µA
		deep power-down mode	[9]	-	0.007	-	µA
RESET pin							
V_{IH}	HIGH-level input voltage		[8]	0.8 × (V_{ps} – 0.35)	-	5.5	V
V_{IL}	LOW-level input voltage		[8]	–0.5	-	0.3 × (V_{ps} – 0.1)	V
V_{hys}	hysteresis voltage		[8]	0.05 × (V_{ps} – 0.35)	-	-	V
Standard I/O pins - normal drive strength							
C_I	input capacitance			-	-	2	pF
I_{IL}	LOW-level input current	V_I = 0 V; on-chip pull-up resistor disabled		-	3	-	nA
I_{IH}	HIGH-level input current	$V_I = V_{DD(IO)}$; on-chip pull-down resistor disabled		-	–3	-	nA
		V_I = 5 V		-	<tbd>	-	nA
I_{OZ}	OFF-state output current	V_O = 0 V to $V_{DD(IO)}$; on-chip pull-up/down resistors disabled; absolute value		-	3	-	nA
V_I	input voltage	pin configured to provide a digital function; $V_{DD(IO)} \geq 2.2$ V		0	-	5.5	V
		$V_{DD(IO)}$ = 0 V		0	-	3.6	V
V_O	output voltage	output active		0	-	$V_{DD(IO)}$	V
V_{IH}	HIGH-level input voltage			0.7 × $V_{DD(IO)}$	-	5.5	V
V_{IL}	LOW-level input voltage			–0.5	-	0.3 × $V_{DD(IO)}$	V
V_{hys}	hysteresis voltage			0.1 × $V_{DD(IO)}$	-	-	V
V_{OH}	HIGH-level output voltage	I_{OH} = –6 mA		$V_{DD(IO)}$ – 0.4	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 6 mA		-	-	0.4	V
I_{OH}	HIGH-level output current	$V_{OH} = V_{DD(IO)}$ – 0.4 V		–6	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V		6	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	drive HIGH; connected to ground	[10]	-	-	86.5	mA
I_{OLS}	LOW-level short-circuit output current	drive LOW; connected to $V_{DD(IO)}$	[10]	-	-	76.5	mA

Table 8. Static characteristics *…continued*
T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
I_{pd}	pull-down current	V_I = 5 V	[12] [13] [14]	-	93	-	µA
I_{pu}	pull-up current	V_I = 0 V	[12] [13] [14]	-	−62	-	µA
		$V_{DD(IO)} < V_I \leq 5$ V		-	10	-	µA
R_s	series resistance	on I/O pins with analog function; analog function enabled			200		Ω
I/O pins - high drive strength							
C_I	input capacitance			-	-	2	pF
I_{IL}	LOW-level input current	V_I = 0 V; on-chip pull-up resistor disabled		-	3	-	nA
I_{IH}	HIGH-level input current	$V_I = V_{DD(IO)}$; on-chip pull-down resistor disabled		-	−3	-	nA
		V_I = 5 V		-	<tbd>	-	nA
I_{OZ}	OFF-state output current	V_O = 0 V to $V_{DD(IO)}$; on-chip pull-up/down resistors disabled; absolute value		-	3	-	nA
V_I	input voltage	pin configured to provide a digital function;					
		$V_{DD(IO)} \geq 2.2$ V		0	-	5.5	V
		$V_{DD(IO)}$ = 0 V		0	-	3.6	V
V_O	output voltage	output active		0	-	$V_{DD(IO)}$	V
V_{IH}	HIGH-level input voltage			0.7 × $V_{DD(IO)}$	-	5.5	V
V_{IL}	LOW-level input voltage			−0.5	-	0.3 × $V_{DD(IO)}$	V
V_{hys}	hysteresis voltage			0.1 × $V_{DD(IO)}$	-	-	V
I_{pd}	pull-down current	$V_I = V_{DD(IO)}$	[12] [13] [14]	-	62	-	µA
I_{pu}	pull-up current	V_I = 0 V	[12] [13] [14]	-	−62	-	µA
		$V_{DD(IO)} < V_I \leq 5$ V		-	10	-	µA
I/O pins - high drive strength: standard drive mode							
I_{OH}	HIGH-level output current	$V_{OH} = V_{DD(IO)} - 0.4$ V		−4	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V		4	-	-	mA

Table 8. Static characteristics *…continued*

T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
I_{OHS}	HIGH-level short-circuit output current	drive HIGH; connected to ground	[10] [13]	-	-	32	mA
I_{OLS}	LOW-level short-circuit output current	drive LOW; connected to $V_{DD(IO)}$	[10] [13]	-	-	32	mA
I/O pins - high drive strength: medium drive mode							
I_{OH}	HIGH-level output current	$V_{OH} = V_{DD(IO)} - 0.4$ V		−8	-	-	mA
I_{OL}	LOW-level output current	$V_{OL} = 0.4$ V		8	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	drive HIGH; connected to ground	[10] [13]	-	-	65	mA
I_{OLS}	LOW-level short-circuit output current	drive LOW; connected to $V_{DD(IO)}$	[10] [13]	-	-	63	mA
I/O pins - high drive strength: high drive mode							
I_{OH}	HIGH-level output current	$V_{OH} = V_{DD(IO)} - 0.4$ V		−14	-	-	mA
I_{OL}	LOW-level output current	$V_{OL} = 0.4$ V		14	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	drive HIGH; connected to ground	[10] [13]	-	-	113	mA
I_{OLS}	LOW-level short-circuit output current	drive LOW; connected to $V_{DD(IO)}$	[10] [13]	-	-	110	mA
I/O pins - high drive strength: ultra-high drive mode							
I_{OH}	HIGH-level output current	$V_{OH} = V_{DD(IO)} - 0.4$ V		−20	-	-	mA
I_{OL}	LOW-level output current	$V_{OL} = 0.4$ V		20	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	drive HIGH; connected to ground	[10] [13]	-	-	165	mA
I_{OLS}	LOW-level short-circuit output current	drive LOW; connected to $V_{DD(IO)}$	[10] [13]	-	-	156	mA
I/O pins - high-speed							
C_I	input capacitance			-	-	2	pF
I_{IL}	LOW-level input current	$V_I = 0$ V; on-chip pull-up resistor disabled		-	3	-	nA
I_{IH}	HIGH-level input current	$V_I = V_{DD(IO)}$; on-chip pull-down resistor disabled		-	−3	-	nA
		$V_I = 5$ V		-	<tbd>	-	nA
I_{OZ}	OFF-state output current	$V_O = 0$ V to $V_{DD(IO)}$; on-chip pull-up/down resistors disabled; absolute value		-	3	-	nA

Table 8. Static characteristics *…continued*

T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
V_I	input voltage	pin configured to provide a digital function;				
		$V_{DD(IO)} \geq 2.2$ V	0	-	5.5	V
		$V_{DD(IO)} = 0$ V	0	-	3.6	V
V_O	output voltage	output active	0	-	$V_{DD(IO)}$	V
V_{IH}	HIGH-level input voltage		0.7 × $V_{DD(IO)}$	-	5.5	V
V_{IL}	LOW-level input voltage		−0.5	-	0.3 × $V_{DD(IO)}$	V
V_{hys}	hysteresis voltage		0.1 × $V_{DD(IO)}$	-	-	V
V_{OH}	HIGH-level output voltage	$I_{OH} = -8$ mA	$V_{DD(IO)} - 0.4$	-	-	V
V_{OL}	LOW-level output voltage	$I_{OL} = 8$ mA	-	-	0.4	V
I_{OH}	HIGH-level output current	$V_{OH} = V_{DD(IO)} - 0.4$ V	−8	-	-	mA
I_{OL}	LOW-level output current	$V_{OL} = 0.4$ V	8	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	drive HIGH; connected to ground [10]	-	-	86	mA
I_{OLS}	LOW-level short-circuit output current	drive LOW; connected to $V_{DD(IO)}$ [10]	-	-	76	mA
I_{pd}	pull-down current	$V_I = V_{DD(IO)}$ [12] [13] [14]	-	62	-	µA
I_{pu}	pull-up current	$V_I = 0$ V [12] [13] [14]	-	−62	-	µA
		$V_{DD(IO)} < V_I \leq 5$ V	-	0	-	µA
Open-drain I^{2}C0-bus pins						
V_{IH}	HIGH-level input voltage		0.7 × $V_{DD(IO)}$	-	-	V
V_{IL}	LOW-level input voltage		−0.5	0.14	0.3 × $V_{DD(IO)}$	V
V_{hys}	hysteresis voltage		0.1 × $V_{DD(IO)}$	-	-	V
V_{OL}	LOW-level output voltage	$I_{OLS} = 3$ mA	-	-	0.4	V
I_{LI}	input leakage current	$V_I = V_{DD(IO)}$ [11]	-	4.5	-	µA
		$V_I = 5$ V	-	-	10	µA
Oscillator pins						
$V_{i(XTAL1)}$	input voltage on pin XTAL1		−0.5	-	1.2	V

Table 8. Static characteristics *…continued*

T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
$V_{o(XTAL2)}$	output voltage on pin XTAL2		−0.5	-	1.2	V
C_{io}	input/output capacitance	[15]	-	-	0.8	pF

Table 8. Static characteristics *…continued*

T_{amb} = –40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
USB0 pins[16]							
V_I	input voltage	on pins USB0_DP; USB0_DM; USB0_VBUS					
		$V_{DD(IO)} \geq 2.2$ V		0	-	5.5	V
		$V_{DD(IO)} = 0$ V		0	-	3.6	V
R_{pd}	pull-down resistance	on pin USB0_VBUS		48	64	80	kΩ
V_{IC}	common-mode input voltage	high-speed mode		–50	200	500	mV
		full-speed/low-speed mode		800	-	2500	mV
		chirp mode		–50	-	600	mV
$V_{i(dif)}$	differential input voltage			100	400	1100	mV
USB1 pins (USB1_DP/USB1_DM)[16]							
I_{OZ}	OFF-state output current	0 V < V_I < 3.3 V	[16]	-	-	±10	μA
V_{BUS}	bus supply voltage		[17]	-	-	5.25	V
V_{DI}	differential input sensitivity voltage	$\lvert(D+) - (D-)\rvert$		0.2	-	-	V
V_{CM}	differential common mode voltage range	includes V_{DI} range		0.8	-	2.5	V
$V_{th(rs)se}$	single-ended receiver switching threshold voltage			0.8	-	2.0	V
V_{OL}	LOW-level output voltage for low-/full-speed	R_L of 1.5 kΩ to 3.6 V		-	-	0.18	V
V_{OH}	HIGH-level output voltage (driven) for low-/full-speed	R_L of 15 kΩ to GND		2.8	-	3.5	V
C_{trans}	transceiver capacitance	pin to GND		-	-	20	pF
Z_{DRV}	driver output impedance for driver which is not high-speed capable	with 33 Ω series resistor; steady state drive	[18]	36	-	44.1	Ω

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] For flash read operations, 2.2 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V; for flash erase/program operations 2.7 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V.

[3] Pin VPP should either be not connected (when OTP does not need to be programmed) or tied to pins VDDIO and VDDREG to ensure the same ramp-up time for both supply voltages.

[4] $V_{DD(REG)(3V3)} = V_{DD(IO)} = V_{DDA(3V3)}$ = 3.3 V; T_{amb} = 25 °C for all power consumption measurements.

[5] PLL1 disabled. Normal power mode.

[6] PLL1 enabled. Normal power mode.

[7] On pin VBAT; T_{amb} = 25 °C. $V_{DD(REG)(3V3)}$ not present.

[8] V_{ps} corresponds to the output of the power switch (see Figure 8) which is determined by the greater of V_{BAT} and $V_{DD(Reg)(3V3)}$.

[9] $V_{DDA(3V3)}$ = 3.3 V; T_{amb} = 25 °C.

[10] Allowed as long as the current limit does not exceed the maximum current allowed by the device.

[11] To V_{SS}.

[12] The values specified are simulated and absolute values.

[13] The weak pull-up resistor is connected to the $V_{DD(IO)}$ rail and pulls up the I/O pin to the $V_{DD(IO)}$ level.

[14] The input cell disables the weak pull-up resistor when the applied input voltage exceeds $V_{DD(IO)}$.

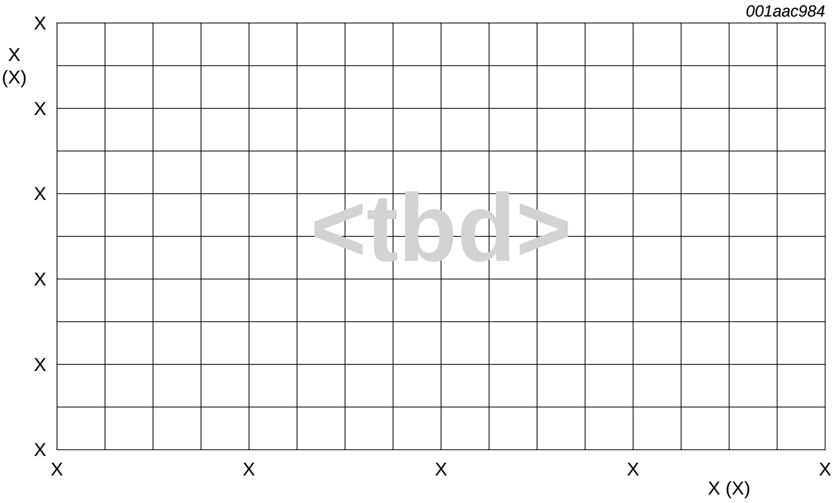
[15] The parameter value specified is a simulated value excluding bond capacitance.

[16] For USB operation 3.0 V $\leq V_{DD((IO)} \leq$ 3.6 V. Guaranteed by design.

[17] $V_{DD(IO)}$ present.

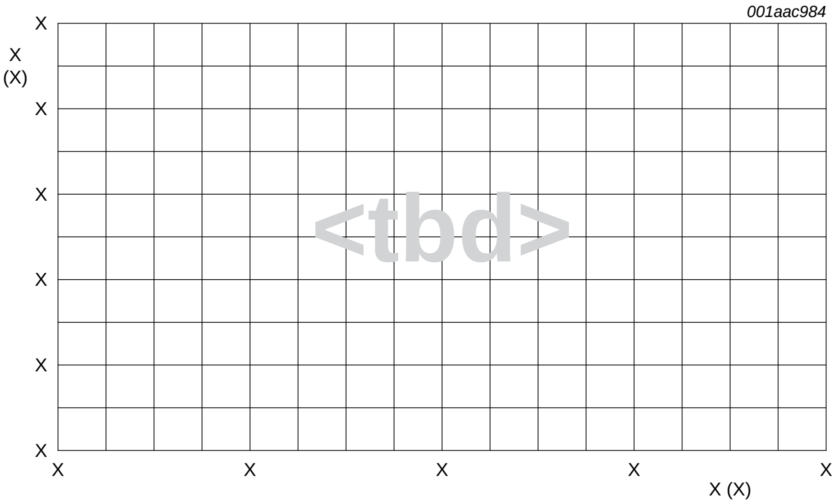
[18] Includes external resistors of 33 Ω ± 1 % on D+ and D–.

10.1 Power consumption



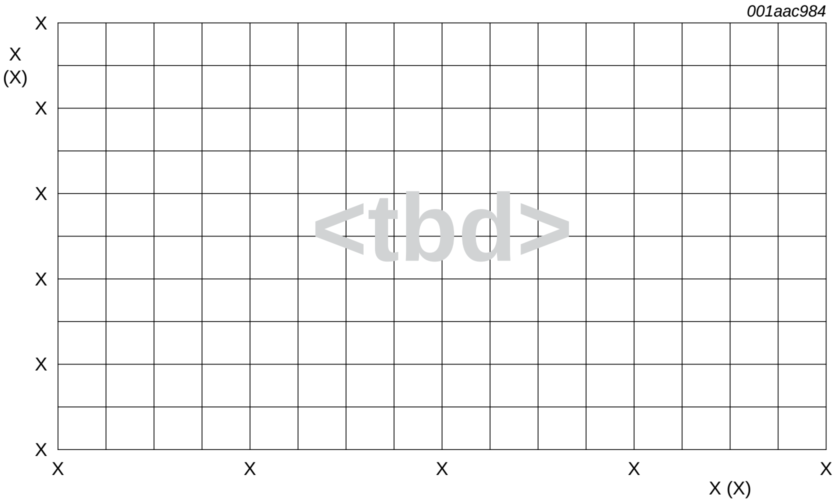
Conditions: T_{amb} = 25 °C; normal mode entered executing code while (1){} from <tbd>; internal pull-up resistors disabled; system PLL enabled; IRC enabled; all peripherals disabled; all peripheral clocks disabled.

Fig 9. Typical supply current versus regulator supply voltage $V_{DD(REEG)(3V3)}$ in active mode



Conditions: $V_{DD(REG)(3V3)}$ = 3.0 V, normal mode entered executing code while (1){} from <tbd>; internal pull-up resistors disabled; system PLL enabled; IRC enabled; all peripherals disabled; all peripheral clocks disabled.

Fig 10. Typical supply current versus temperature in active mode



Conditions: $V_{DD(REG)(3V3)}$ = 3.0 V; internal pull-up resistors disabled; system PLL enabled; IRC enabled; all peripherals disabled; all peripheral clocks disabled.

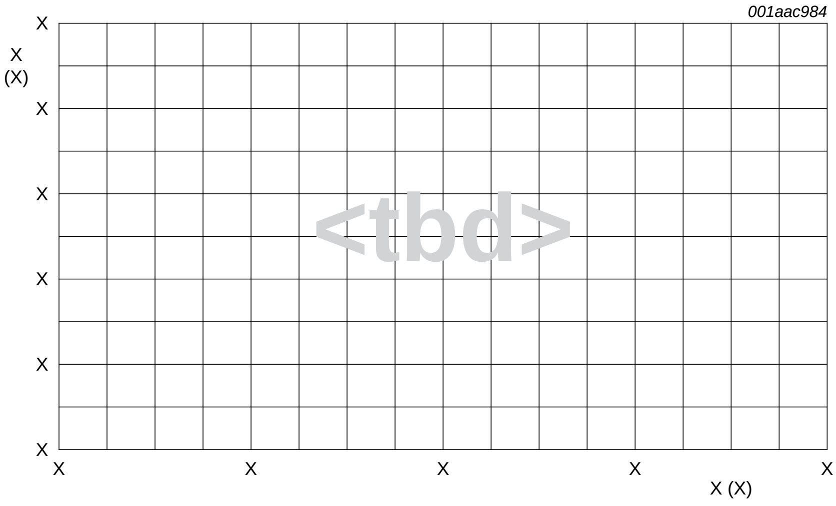
Fig 11. Typical supply current versus temperature in sleep mode

Conditions: V_{BAT} = 0 V; $V_{DD(IO)}$ = 0 V.

Fig 12. Typical supply current versus temperature in Deep-sleep mode

Conditions: V_{BAT} = 0 V; $V_{DD(IO)}$ = 0 V.

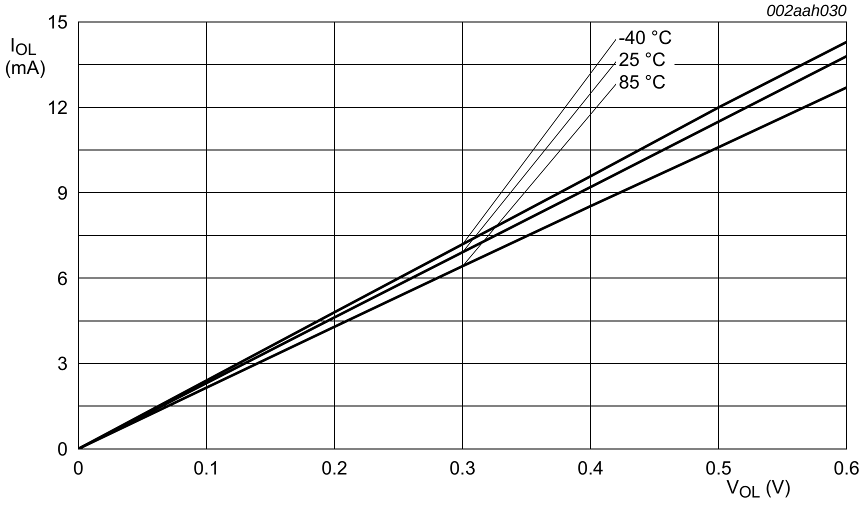
Fig 13. Typical supply current versus temperature in Power-down mode



Conditions: V_{BAT} = 0 V; $V_{DD(IO)}$ = 0 V.

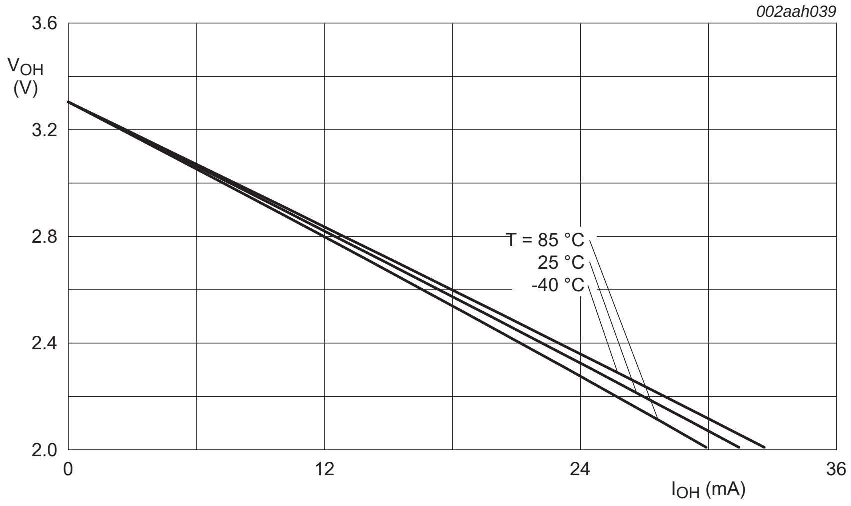
Fig 14. Typical supply current versus temperature in Deep power-down mode

10.2 Electrical pin characteristics



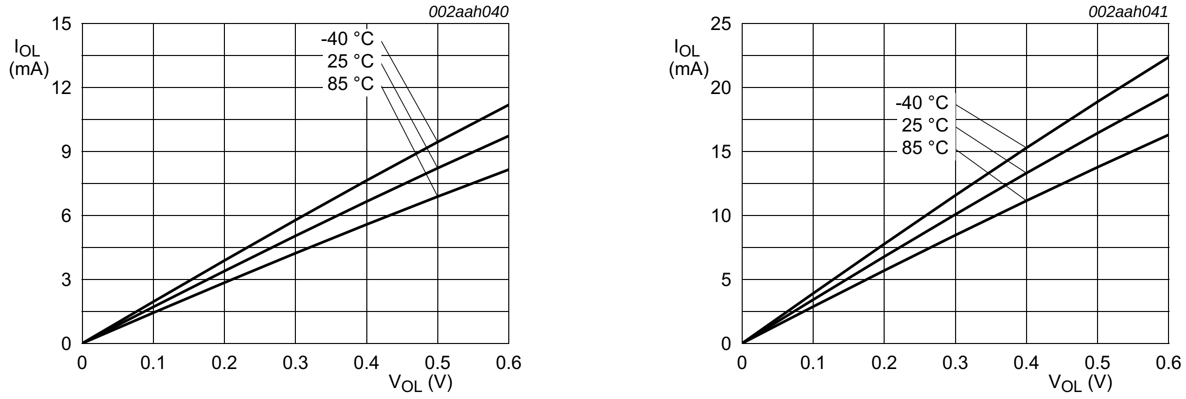
Conditions: $V_{DD(REG)(3V3)}$ = $V_{DD(IO)}$ = 3.3 V.

Fig 15. Normal-drive pins; typical LOW level output current I_{OL} versus LOW level output voltage V_{OL}



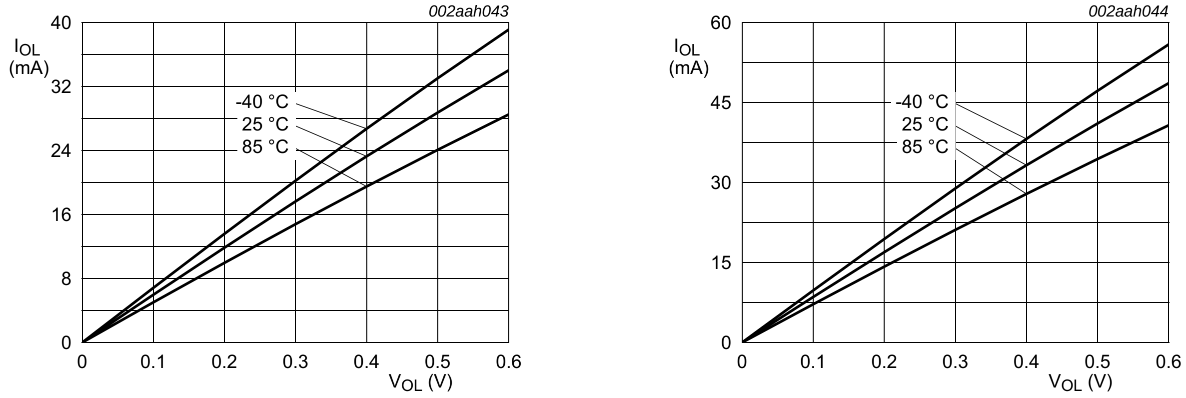
Conditions: $V_{DD(REG)(3V3)} = V_{DD(IO)} = 3.3$ V.

Fig 16. Normal-drive pins; typical HIGH level output voltage V_{OL} versus HGH level output current I_{OH}



Conditions: $V_{DD(REG)(3V3)} = V_{DD(IO)} = 3.3$ V; normal-drive; EHD = 0x0.

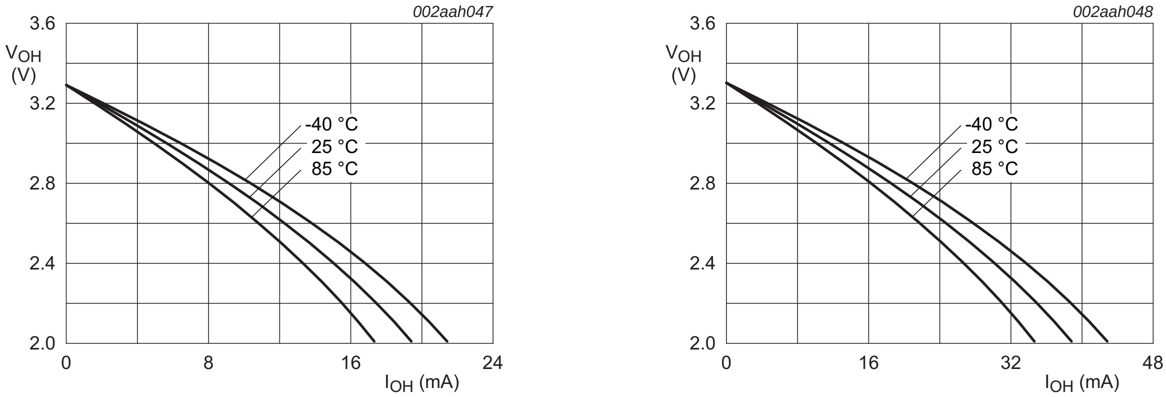
Conditions: $V_{DD(REG)(3V3)} = V_{DD(IO)} = 3.3$ V; medium-drive; EHD = 0x1.



Conditions: $V_{DD(REG)(3V3)} = V_{DD(IO)} = 3.3$ V; high-drive; EHD = 0x2.

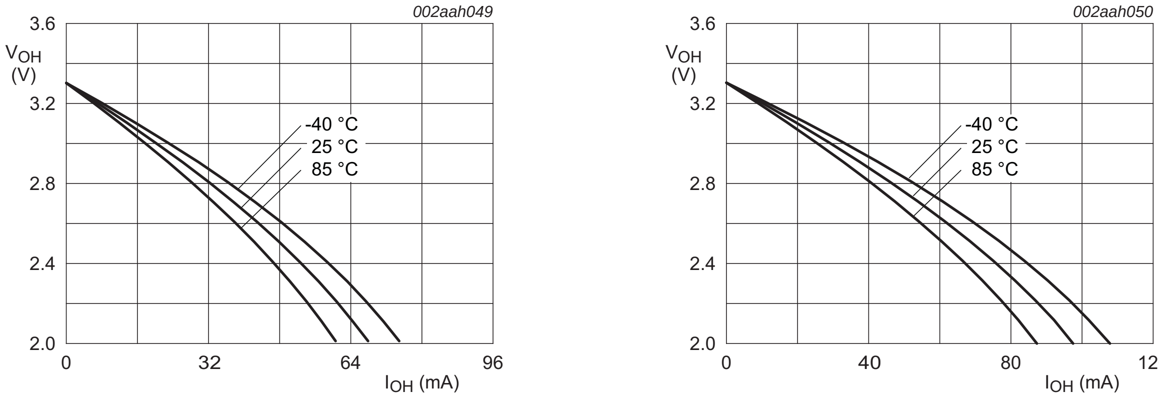
Conditions: $V_{DD(REG)(3V3)} = V_{DD(IO)} = 3.3$ V; ultra high-drive; EHD = 0x3.

Fig 17. High-drive pins; typical LOW level output current I_{OL} versus LOW level output voltage V_{OL}



Conditions: $V_{DD(REG)(3V3)} = V_{DD(IO)} = 3.3$ V; normal-drive; EHD = 0x0.

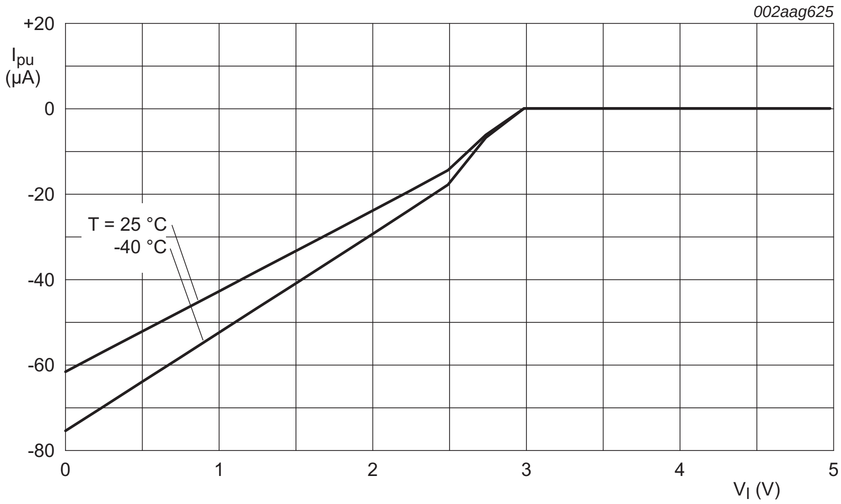
Conditions: $V_{DD(REG)(3V3)} = V_{DD(IO)} = 3.3$ V; medium-drive; EHD = 0x1.



Conditions: $V_{DD(REG)(3V3)} = V_{DD(IO)} = 3.3$ V; high-drive; EHD = 0x2.

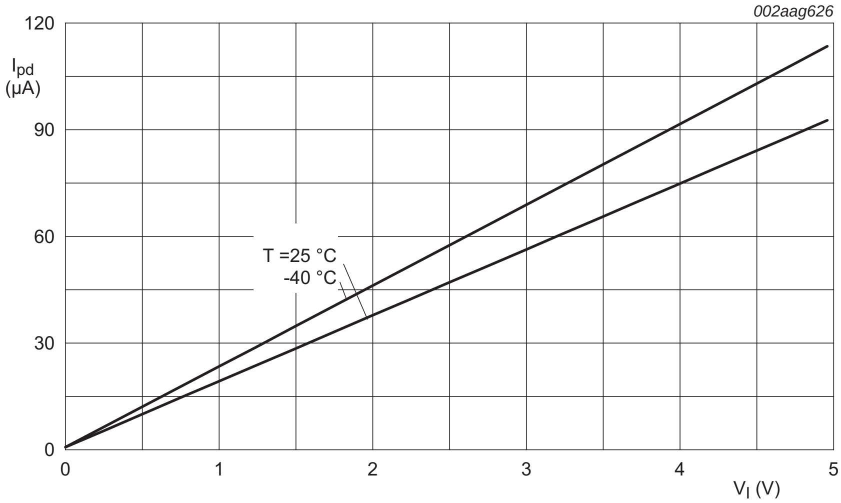
Conditions: $V_{DD(REG)(3V3)} = V_{DD(IO)} = 3.3$ V; ultra high-drive; EHD = 0x3.

Fig 18. High-drive pins; typical HIGH level output voltage V_{OH} versus HGH level output current I_{OH}



Conditions: $V_{DD(IO)}$ = 3.3 V. Simulated data. Values at T = 25 °C are typical values. Values at T = –40 °C correspond to minimum values.

Fig 19. Typical pull-up current I_{pu} versus input voltage V_I



Conditions: $V_{DD(IO)}$ = 3.3 V. Simulated data. Values at T = 25 °C are typical values. Values at T = -40 °C correspond to maximum values.

Fig 20. Typical pull-down current I_{pd} versus input voltage V_I

10.3 BOD static characteristics

Table 9. BOD static characteristics[1]

T_{amb} = 25 °C; simulated values for nominal processing.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{th}	threshold voltage	interrupt level 0				
		assertion	-	2.25	-	V
		de-assertion	-	<tbd>	-	V
		interrupt level 1				
		assertion	-	2.35	-	V
		de-assertion	-	<tbd>	-	V
		interrupt level 2				
		assertion	-	2.95	-	V
		de-assertion	-	<tbd>	-	V
		interrupt level 3				
		assertion	-	3.05	-	V
		de-assertion	-	<tbd>	-	V
		reset level 0				
		assertion	-	1.9	-	V
		de-assertion	-	<tbd>	-	V
		reset level 1				
		assertion	-	2.0	-	V
		de-assertion	-	<tbd>	-	V
		reset level 2				
		assertion	-	2.1	-	V
		de-assertion	-	<tbd>	-	V
		reset level 3				
		assertion	-	2.2	-	V
		de-assertion	-	<tbd>	-	V

[1] Interrupt and reset levels are selected by writing to the BODLV1/2 bits in the control register CREGE0, see *the LPC18xx user manual*.

11. Dynamic characteristics

11.1 Flash/EEPROM memory

Table 10. Flash characteristics

T_{amb} = −40 °C to +85 °C, unless otherwise specified. $V_{DD(REG)(3V3)}$ = 2,2 V to 3.6 V for read operations; $V_{DD(REG)(3V3)}$ = 2.7 V to 3.6 V for erase/program operations.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
N_{endu}	endurance	sector erase/program	[1]	10000	-	-	cycles
		page erase/program; page in large sector		1000	-	-	cycles
		page erase/program; page in small sector		10000	-	-	cycles
t_{ret}	retention time	powered		10	-	-	years
		unpowered		10	-	-	years
t_{er}	erase time	page, sector, or multiple consecutive sectors		-	50	-	ms
t_{prog}	programming time		[2]	-	1	-	ms

[1] Number of erase/program cycles.

[2] Programming times are given for writing 512 bytes from RAM to the flash. Data must be written to the flash in blocks of 512 bytes.

Table 11. EEPROM characteristics

T_{amb} = −40 °C to +85 °C; $V_{DD(REG)(3V3)}$ = 2.7 V to 3.6 V.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{clk}	clock frequency			800	1500	1600	kHz
N_{endu}	endurance			100 000	<tbd>	-	cycles
t_{ret}	retention time			-	20	-	years
t_a	access time	read		-	120	-	ns
		erase/program; f_{clk} = 1500 kHz		-	1.99	-	ms
		erase/program; f_{clk} = 1600 kHz		-	1.87	-	ms
t_{wait}	wait time	read; RPHASE1	[1]	35	-	-	ns
		read; RPHASE2	[1]	70	-	-	ns
		write; PHASE1	[1]	20	-	-	ns
		write; PHASE2	[1]	40	-	-	ns
		write; PHASE3	[1]	10	-	-	ns

[1] See the LPC18xx user manual how to program the wait states for the different read (RPHASEx) and erase/program phases (PHASEx)

11.2 Wake-up times

Table 12. Dynamic characteristic: Wake-up from Deep-sleep, Power-down, and Deep power-down modes

T_{amb} = −40 °C to +85 °C

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
t_{wake}	wake-up time	from Sleep mode [2]	<tbd>	5 × $T_{cy(clk)}$	-	ns
		from Deep-sleep and Power-down mode	12	51	-	μs
		from Deep power-down mode	<tbd>	<tbd>	-	ns
		after reset	<tbd>	<tbd>	-	ns

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] $T_{cy(clk)}$ = 1/CCLK with CCLK = CPU clock frequency.

11.3 External clock

Table 13. Dynamic characteristic: external clock

T_{amb} = −40 °C to +85 °C; $V_{DD(IO)}$ over specified ranges.[1]

Symbol	Parameter	Conditions	Min	Typ[2]	Max	Unit
f_{osc}	oscillator frequency		1	-	25	MHz
$T_{cy(clk)}$	clock cycle time		40	-	1000	ns
t_{CHCX}	clock HIGH time		$T_{cy(clk)}$ × <tbd>	-	-	ns
t_{CLCX}	clock LOW time		$T_{cy(clk)}$ × <tbd>	-	-	ns
t_{CLCH}	clock rise time		-	-	<tbd>	ns
t_{CHCL}	clock fall time		-	-	<tbd>	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

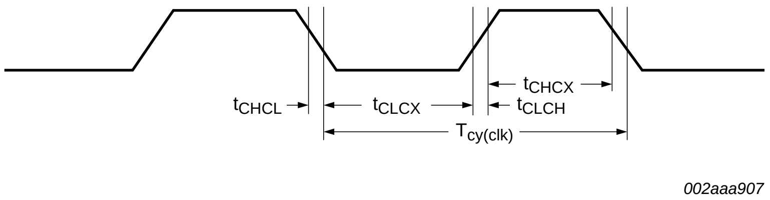


Fig 21. External clock timing (with an amplitude of at least $V_{i(RMS)}$ = 200 mV)

11.4 Crystal oscillator

Table 14. Dynamic characteristic: oscillator

T_{amb} = −40 °C to +85 °C; $V_{DD(IO)}$ over specified ranges; 2.2 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V.[1]

Symbol	Parameter	Conditions		Min	Typ[2]	Max	Unit
Low-frequency mode (1-20 MHz)[5]							
$t_{jit(per)}$	period jitter time	5 MHz crystal	[3][4]	-	13.2	-	ps
		10 MHz crystal		-	6.6	-	ps
		15 MHz crystal		-	4.8	-	ps
High-frequency mode (20 - 25 MHz)[6]							
$t_{jit(per)}$	period jitter time	20 MHz crystal	[3][4]	-	4.3	-	ps
		25 MHz crystal		-	3.7	-	ps

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[3] Indicates RMS period jitter.

[4] PLL-induced jitter is not included.

[5] Select HF = 0 in the XTAL_OSC_CTRL register.

[6] Select HF = 1 in the XTAL_OSC_CTRL register.

11.5 IRC oscillator

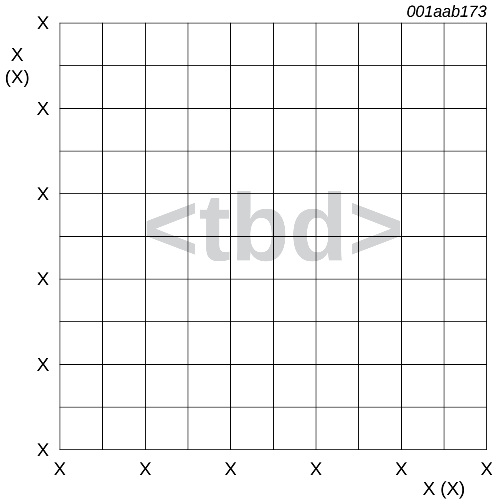
Table 15. Dynamic characteristic: IRC oscillator

T_{amb} = −40 °C to +85 °C; 2.2 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V.[1]

Symbol	Parameter	Conditions	Min	Typ[2]	Max	Unit
$f_{osc(RC)}$	internal RC oscillator frequency	-	11.88	12.0	12.12	MHz

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.



Conditions: Frequency values are typical values.

Fig 22. Internal RC oscillator frequency versus temperature

11.6 RTC oscillator

Table 16. Dynamic characteristic: RTC oscillator

$T_{amb} = -40$ °C to +85 °C; $2.2\ V \leq V_{DD(REG)(3V3)} \leq 3.6\ V$ or $2.2\ V \leq V_{BAT} \leq 3.6\ V$[1]

Symbol	Parameter	Conditions	Min	Typ[2]	Max	Unit
$f_{i(RTC)}$	RTC input frequency	-	-	32.768	-	kHz
$I_{DD(RTC)}$	RTC supply current			280	800	nA

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

11.7 I²C-bus

Table 17. Dynamic characteristic: I²C-bus pins

$T_{amb} = -40$ °C to +85 °C; $2.2\ V \leq V_{DD(REG)(3V3)} \leq 3.6\ V$.[1]

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCL}	SCL clock frequency	Standard-mode	0	100	kHz
		Fast-mode	0	400	kHz
		Fast-mode Plus	0	1	MHz
t_f	fall time [3][4][5][6]	of both SDA and SCL signals Standard-mode	-	300	ns
		Fast-mode	$20 + 0.1 \times C_b$	300	ns
		Fast-mode Plus	-	120	ns
t_{LOW}	LOW period of the SCL clock	Standard-mode	4.7	-	µs
		Fast-mode	1.3	-	µs
		Fast-mode Plus	0.5	-	µs

Table 17. Dynamic characteristic: I^{2}C-bus pins

T_{amb} = −40 °C to +85 °C; 2.2 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V.[1]

Symbol	Parameter		Conditions	Min	Max	Unit
t_{HIGH}	HIGH period of the SCL clock		Standard-mode	4.0	-	µs
			Fast-mode	0.6	-	µs
			Fast-mode Plus	0.26	-	µs
$t_{HD;DAT}$	data hold time	[2][3][7]	Standard-mode	0	-	µs
			Fast-mode	0	-	µs
			Fast-mode Plus	0	-	µs
$t_{SU;DAT}$	data set-up time	[8][9]	Standard-mode	250	-	ns
			Fast-mode	100	-	ns
			Fast-mode Plus	50	-	ns

[1] Parameters are valid over operating temperature range unless otherwise specified. See the I^{2}C-bus specification *UM10204* for details.

[2] tHD;DAT is the data hold time that is measured from the falling edge of SCL; applies to data in transmission and the acknowledge.

[3] A device must internally provide a hold time of at least 300 ns for the SDA signal (with respect to the V_{IH}(min) of the SCL signal) to bridge the undefined region of the falling edge of SCL.

[4] C_b = total capacitance of one bus line in pF. If mixed with Hs-mode devices, faster fall times are allowed.

[5] The maximum t_f for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time for the SDA output stage t_f is specified at 250 ns. This allows series protection resistors to be connected in between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_f.

[6] In Fast-mode Plus, fall time is specified the same for both output stage and bus timing. If series resistors are used, designers should allow for this when considering bus timing.

[7] The maximum $t_{HD;DAT}$ could be 3.45 µs and 0.9 µs for Standard-mode and Fast-mode but must be less than the maximum of $t_{VD;DAT}$ or $t_{VD;ACK}$ by a transition time. This maximum must only be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal. If the clock stretches the SCL, the data must be valid by the set-up time before it releases the clock.

[8] tSU;DAT is the data set-up time that is measured with respect to the rising edge of SCL; applies to data in transmission and the acknowledge.

[9] A Fast-mode I^{2}C-bus device can be used in a Standard-mode I^{2}C-bus system but the requirement $t_{SU;DAT}$ = 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{r(max)}$ + $t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the Standard-mode I^{2}C-bus specification) before the SCL line is released. Also the acknowledge timing must meet this set-up time.

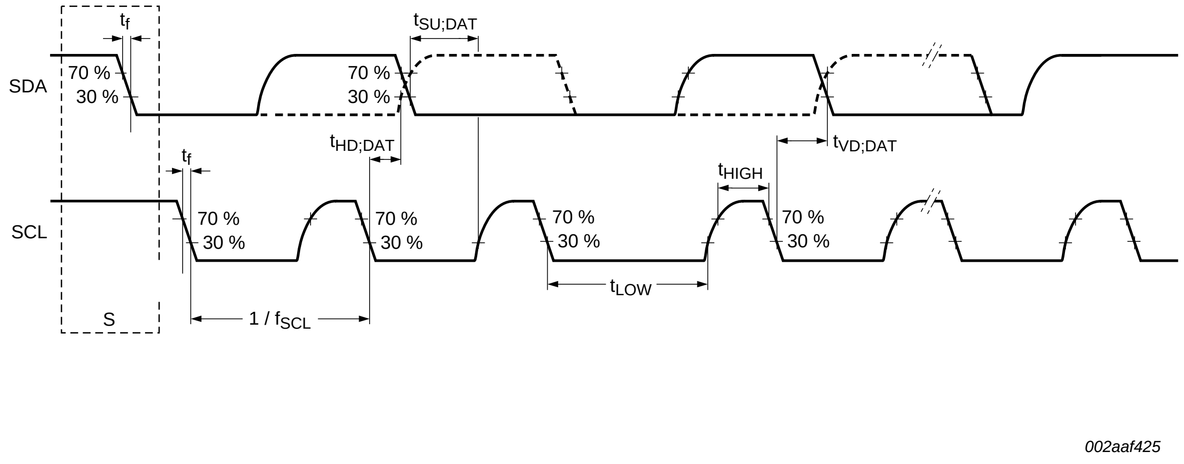


Fig 23. I^{2}C-bus pins clock timing

11.8 I²S-bus interface

Table 18. Dynamic characteristics: I²S-bus interface pins

T_{amb} = 25 °C; 2.2 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V; 2.7 V ≤ $V_{DD(IO)}$ ≤ 3.6 V; C_L = 20 pF. Conditions and data refer to I2S0 and I2S1 pins. Simulated values.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
common to input and output							
t_r	rise time			-	4	-	ns
t_f	fall time			-	4	-	ns
t_{WH}	pulse width HIGH	on pins I2Sx_TX_SCK and I2Sx_RX_SCK		<tbd>	-	-	-
t_{WL}	pulse width LOW	on pins I2Sx_TX_SCK and I2Sx_RX_SCK		-	-	<tbd>	ns
output							
$t_{v(Q)}$	data output valid time	on pin I2Sx_TX_SDA	[1]	-	4.4	-	ns
		on pin I2Sx_TX_WS		-	4.3	-	ns
input							
$t_{su(D)}$	data input set-up time	on pin I2Sx_RX_SDA	[1]	-	0	-	ns
		on pin I2Sx_RX_WS			0.20		ns
$t_{h(D)}$	data input hold time	on pin I2Sx_RX_SDA	[1]	-	3.7	-	ns
		on pin I2Sx_RX_WS		-	3.9	-	ns

[1] Clock to the I²S-bus interface BASE_APB1_CLK = 150 MHz; peripheral clock to the I²S-bus interface PCLK = BASE_APB1_CLK / 12. I²S clock cycle time $T_{cy(clk)}$ = 79.2 ns, corresponds to the SCK signal in the *I²S-bus specification*.

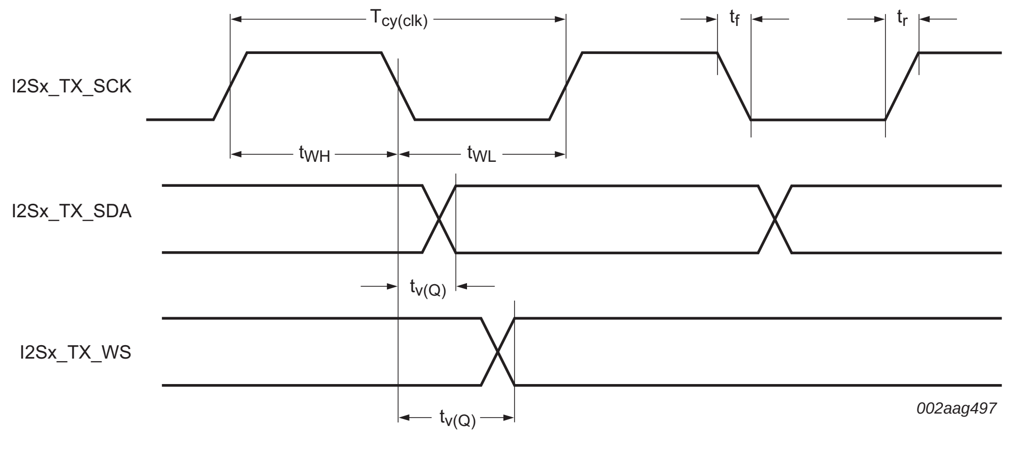


Fig 24. I²S-bus timing (transmit)

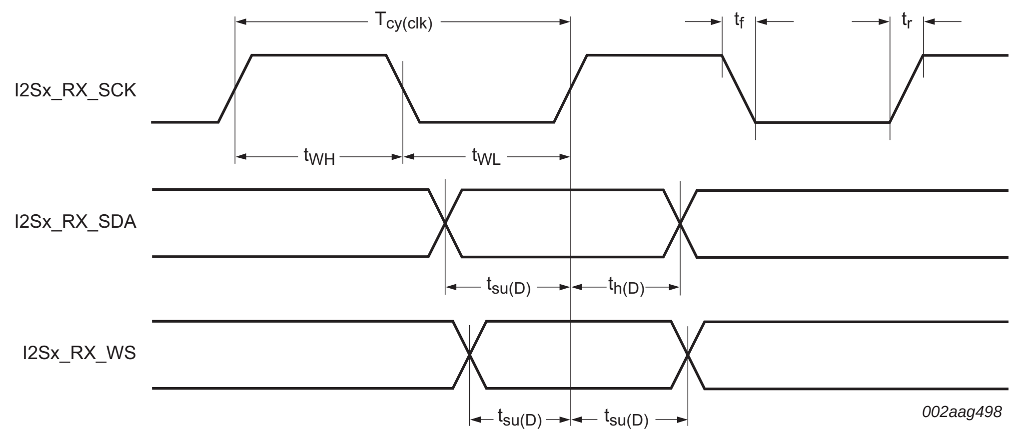


Fig 25. I^2S-bus timing (receive)

11.9 USART interface

Table 19. Dynamic characteristics: USART interface

$T_{amb} = 25$ °C; $2.2\ V \leq V_{DD(REG)(3V3)} \leq 3.6$ V; $2.7\ V \leq V_{DD(IO)} \leq 3.6$ V; $C_L = 20$ pF. Simulated values.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{cy(clk)}$	clock cycle time	on pins Ux_UCLK	-	0.1	-	μs
output						
$t_{v(Q)}$	data output valid time	on pin Ux_TXD	-	6.5	-	ns

11.10 SSP interface

Table 20. Dynamic characteristics: SSP pins in SPI mode

T_{amb} = 25 °C; $V_{DD(REG)(3V3)}$ = 3.3 V. 2.2 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V; 2.7 V ≤ $V_{DD(IO)}$ ≤ 3.6 V. Simulated values.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{cy(clk)}$	clock cycle time	full-duplex mode [1]	-	40	-	ns
		when only transmitting	-	20	-	ns
SSP master						
t_{DS}	data set-up time	in SPI mode	-	8.8	-	ns
t_{DH}	data hold time	in SPI mode	-	–5.0	-	ns
$t_{v(Q)}$	data output valid time	in SPI mode	-	3.9	-	ns
$t_{h(Q)}$	data output hold time	in SPI mode	-	0.4	-	ns
SSP slave						
$T_{cy(PCLK)}$	PCLK cycle time		10			ns
$T_{cy(clk)}$	clock cycle time	[2]	120	-	-	ns
t_{DS}	data set-up time	in SPI mode	10	-	-	ns
t_{DH}	data hold time	in SPI mode	120	-	-	ns
$t_{v(Q)}$	data output valid time	in SPI mode	-	-	<tbd> × $T_{cy(PCLK)}$ + <tbd>	ns
$t_{h(Q)}$	data output hold time	in SPI mode	-	-	<tbd> × $T_{cy(PCLK)}$ + <tbd>	ns

[1] $T_{cy(clk)}$ = (SSPCLKDIV × (1 + SCR) × CPSDVSR) / f_{main}. The clock cycle time derived from the SPI bit rate $T_{cy(clk)}$ is a function of the main clock frequency f_{main}, the SSP peripheral clock divider (SSPCLKDIV), the SSP SCR parameter (specified in the SSP0CR0 register), and the SSP CPSDVSR parameter (specified in the SSP clock prescale register).

[2] $T_{cy(clk)}$ = 12 × $T_{cy(PCLK)}$.

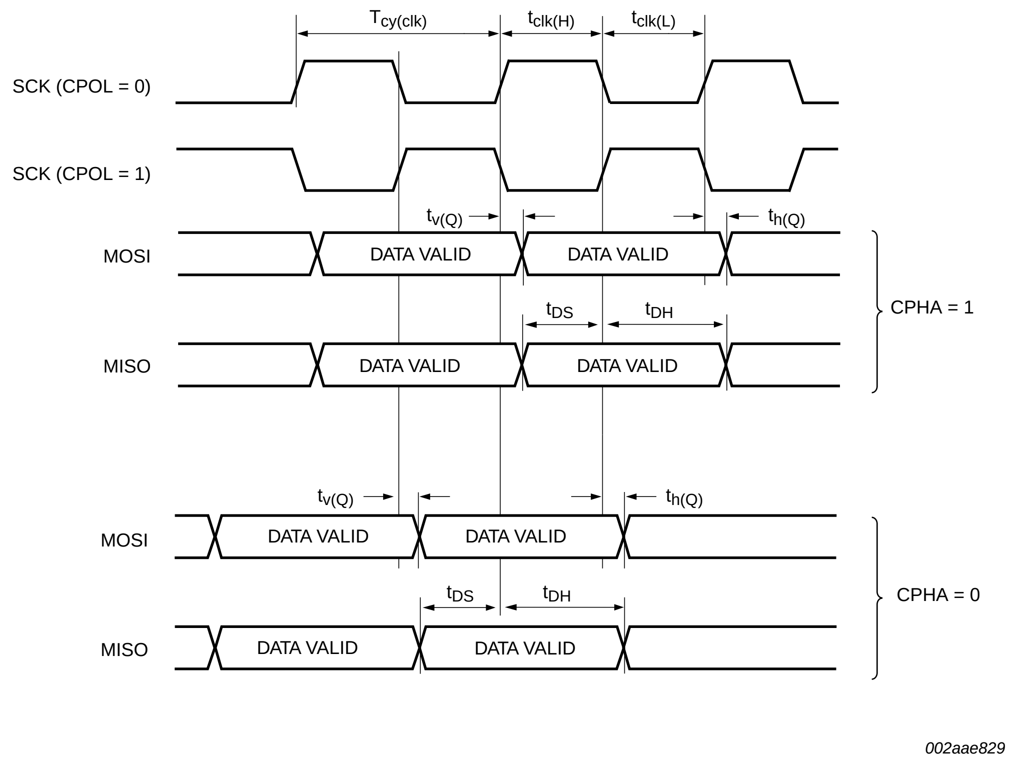


Fig 26. SSP master timing in SPI mode

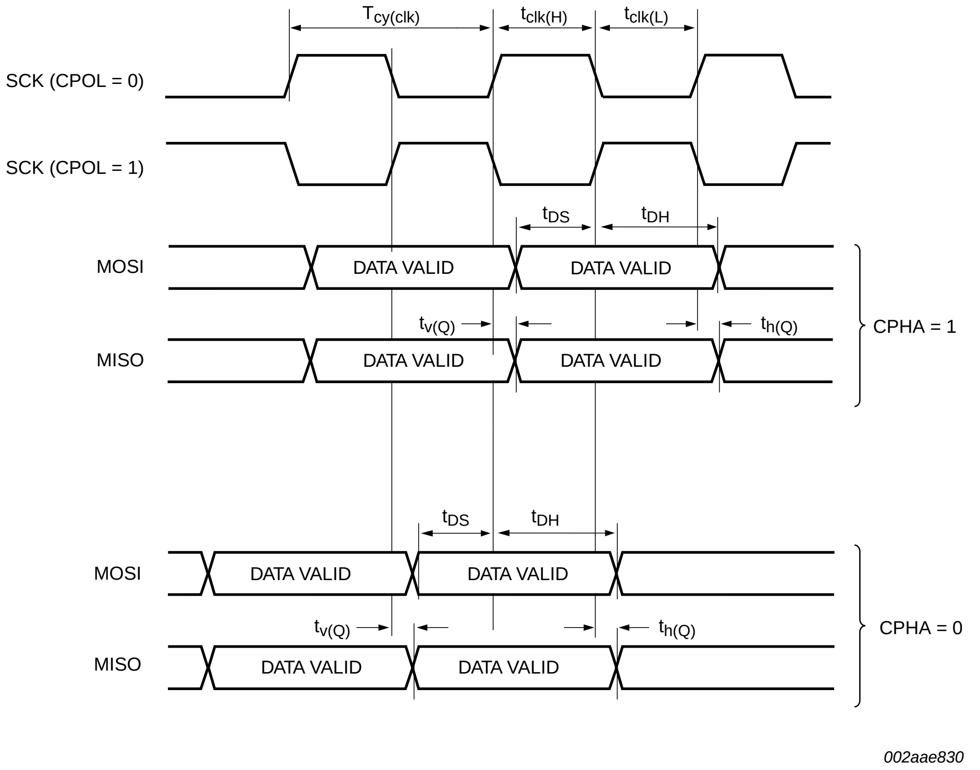


Fig 27. SSP slave timing in SPI mode

11.11 External memory interface

Table 21. Dynamic characteristics: Static external memory interface

C_L = 22 pF for EMC_Dn C_L = 20 pF for all others; T_{amb} = −40 °C to 85 °C; 2.2 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V; 2.7 V ≤ $V_{DD(IO)}$ ≤ 3.6 V; values guaranteed by design.

Symbol	Parameter[1]	Conditions	Min	Typ	Max	Unit
Read cycle parameters						
t_{CSLAV}	$\overline{CS}$ LOW to address valid time		−3.1	-	1.6	ns
t_{CSLOEL}	$\overline{CS}$ LOW to $\overline{OE}$ LOW time	[2]	−0.6 + $T_{cy(clk)}$ × WAITOEN	-	1.3 + $T_{cy(clk)}$ × WAITOEN	ns
$t_{CSLBLSL}$	$\overline{CS}$ LOW to $\overline{BLS}$ LOW time	PB = 1	−0.7	-	1.8	ns
t_{OELOEH}	$\overline{OE}$ LOW to $\overline{OE}$ HIGH time	[2]	−0.6 + (WAITRD − WAITOEN + 1) × $T_{cy(clk)}$	-	−0.4 + (WAITRD − WAITOEN + 1) × $T_{cy(clk)}$	ns
t_{am}	memory access time		-	-	−16 + (WAITRD − WAITOEN +1) × $T_{cy(clk)}$	ns
$t_{h(D)}$	data input hold time		−16	-	-	ns
$t_{CSHBLSH}$	$\overline{CS}$ HIGH to $\overline{BLS}$ HIGH time	PB = 1	−0.4	-	1.9	ns
t_{CSHOEH}	CS HIGH to $\overline{OE}$ HIGH time		−0.4	-	1.4	ns
t_{OEHANV}	$\overline{OE}$ HIGH to address invalid	PB = 1	−2.0	-	2.6	ns
t_{CSHEOR}	$\overline{CS}$ HIGH to end of read time	[3]	−2.0	-	0	ns
t_{CSLSOR}	$\overline{CS}$ LOW to start of read time	[4]	0	-	1.8	ns
Write cycle parameters						
t_{CSLAV}	$\overline{CS}$ LOW to address valid time		−3.1	-	1.6	ns
t_{CSLDV}	$\overline{CS}$ LOW to data valid time		−3.1	-	1.5	ns
t_{CSLWEL}	$\overline{CS}$ LOW to $\overline{WE}$ LOW time	PB = 1	−1.5	-	0.2	ns
$t_{CSLBLSL}$	$\overline{CS}$ LOW to $\overline{BLS}$ LOW time	PB = 1	−0.7	-	1.8	ns
t_{WELWEH}	$\overline{WE}$ LOW to $\overline{WE}$ HIGH time	PB = 1 [2]	−0.6 + (WAITWR − WAITWEN + 1) × $T_{cy(clk)}$	-	−0.4 + (WAITWR − WAITWEN + 1) × $T_{cy(clk)}$	ns
t_{WEHDNV}	$\overline{WE}$ HIGH to data invalid time	PB = 1 [2]	−0.9 + $T_{cy(clk)}$	-	2.3 + $T_{cy(clk)}$	ns
t_{WEHEOW}	$\overline{WE}$ HIGH to end of write time	PB = 1 [2] [5]	−0.4 + $T_{cy(clk)}$	-	−0.3 + $T_{cy(clk)}$	ns
$t_{CSLBLSL}$	$\overline{CS}$ LOW to $\overline{BLS}$ LOW	PB = 0	−0.7	-	1.8	ns
$t_{BLSLBLSH}$	$\overline{BLS}$ LOW to $\overline{BLS}$ HIGH time	PB = 0 [2]	−0.9 + (WAITWR − WAITWEN + 1) × $T_{cy(clk)}$	-	−0.1 + (WAITWR − WAITWEN + 1) × $T_{cy(clk)}$	ns
$t_{BLSHEOW}$	$\overline{BLS}$ HIGH to end of write time	PB = 0 [2] [5]	−1.9 + $T_{cy(clk)}$	-	−0.5 + $T_{cy(clk)}$	ns

Table 21. Dynamic characteristics: Static external memory interface *…continued*

C_L = 22 pF for EMC_Dn C_L = 20 pF for all others; T_{amb} = −40 °C to 85 °C; 2.2 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V; 2.7 V ≤ $V_{DD(IO)}$ ≤ 3.6 V; values guaranteed by design.

Symbol	Parameter[1]	Conditions		Min	Typ	Max	Unit
$t_{BLSHDNV}$	$\overline{\text{BLS}}$ HIGH to data invalid time	PB = 0	[2]	$-2.5 + T_{cy(clk)}$	-	$1.4 + T_{cy(clk)}$	ns
t_{CSHEOW}	$\overline{\text{CS}}$ HIGH to end of write time		[5]	−2.0	-	0	ns
$t_{BLSHDNV}$	$\overline{\text{BLS}}$ HIGH to data invalid time	PB = 1		−2.5	-	1.4	ns
t_{WEHANV}	WE HIGH to address invalid time	PB = 1		$-0.9 + T_{cy(clk)}$	-	$2.4 + T_{cy(clk)}$	ns

[1] Parameters specified for 40 % of $V_{DD(IO)}$ for rising edges and 60 % of $V_{DD(IO)}$ for falling edges.

[2] $T_{cy(clk)}$ = 1/CCLK (see *LPC18xx User manual*).

[3] End Of Read (EOR): longest of t_{CSHOEH}, t_{OEHANV}, $t_{CSHBLSH}$.

[4] Start Of Read (SOR): longest of t_{CSLAV}, t_{CSLOEL}, $t_{CSLBLSL}$.

[5] End Of Write (EOW): earliest of address not valid or $\overline{\text{EMC\_BLSn}}$ HIGH.

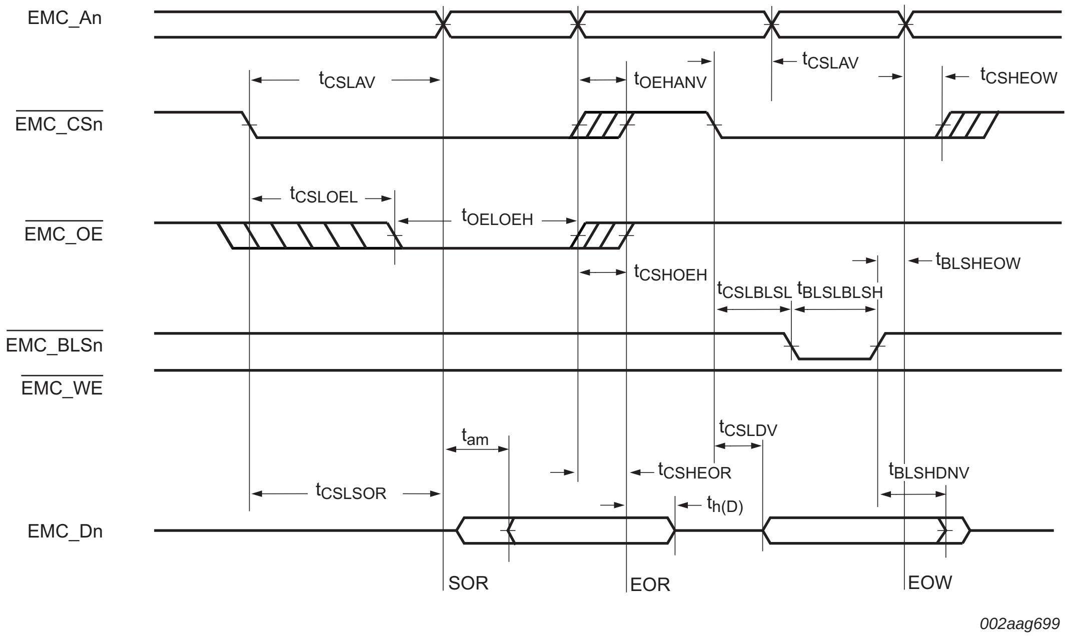


Fig 28. External static memory read/write access (PB = 0)

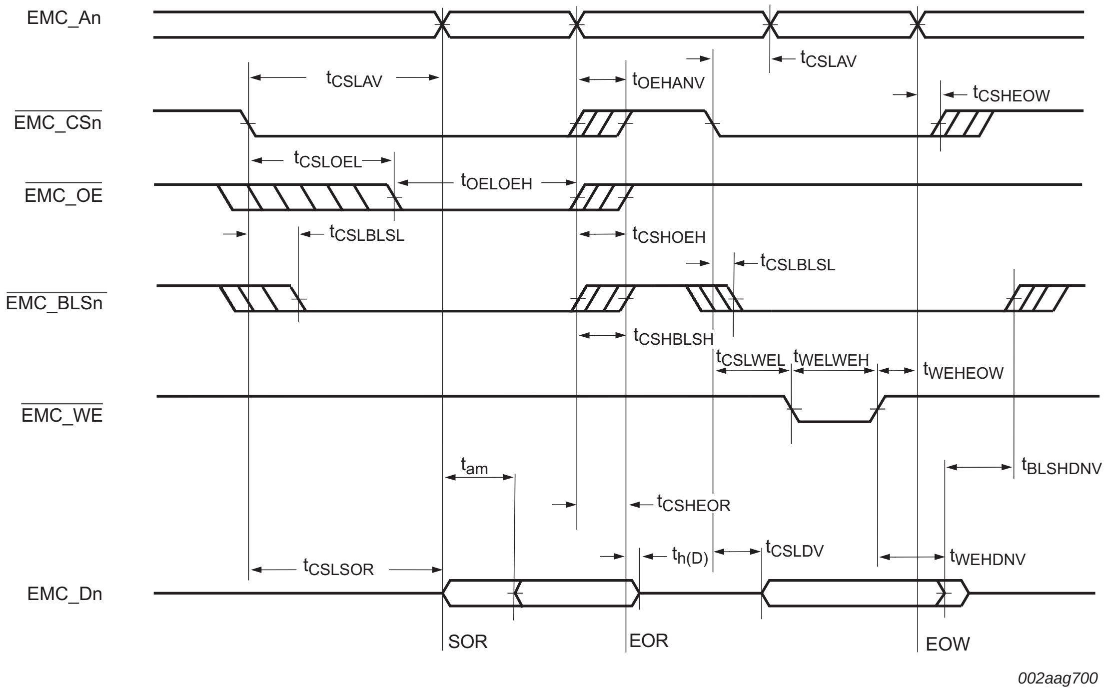


Fig 29. External static memory read/write access (PB = 1)

Table 22. Dynamic characteristics: Dynamic external memory interface

Simulated data over temperature and process range; C_L = 10 pF for $\overline{\text{EMC\_DYCSn}}$, $\overline{\text{EMC\_RAS}}$, $\overline{\text{EMC\_CAS}}$, $\overline{\text{EMC\_WE}}$, EMC_An; C_L = 9 pF for EMC_Dn; C_L = 5 pF for EMC_DQMOUTn, EMC_CLKn, EMC_CKEOUTn; T_{amb} = −40 °C to 85 °C; $2.2\ V \leq V_{DD(REG)(3V3)} \leq 3.6\ V$; $V_{DD(IO)} = 3.3\ V \pm 10\ \%$; RD = 1 (see LPC18xx User manual); EMC_CLKn delays CLK0_DELAY = CLK1_DELAY = CLK2_DELAY = CLK3_DELAY = 0.

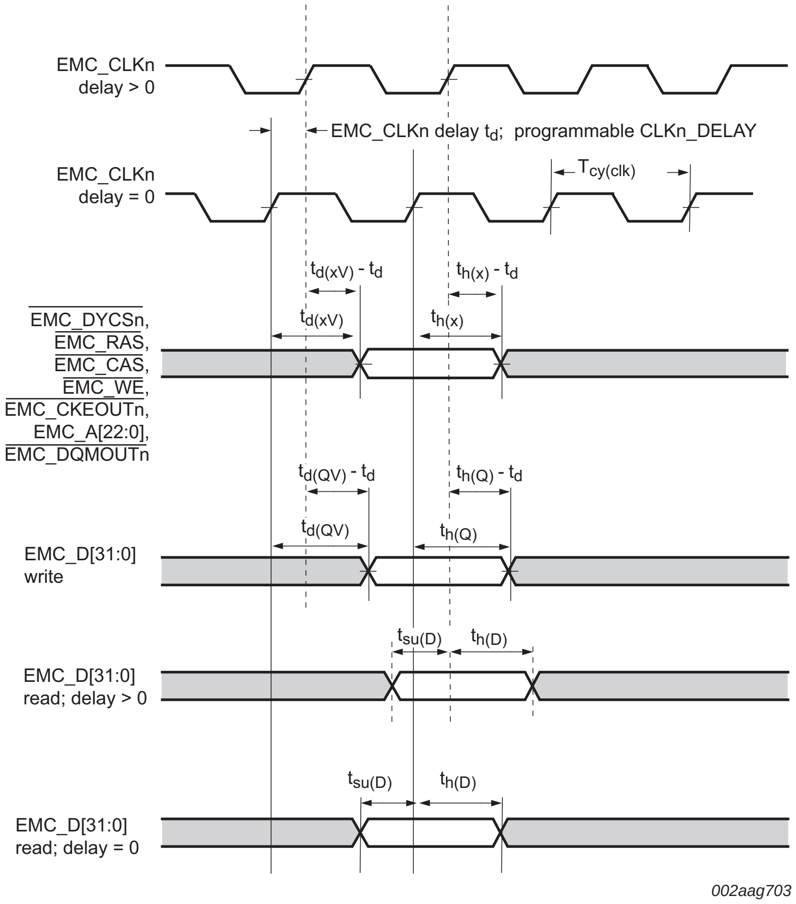
Symbol	Parameter	Min	Typ	Max	Unit
$T_{cy(clk)}$	clock cycle time	8.4	-	-	ns
Common to read and write cycles					
$t_{d(DYCSV)}$	dynamic chip select valid delay time	-	$3.1 + 0.5 \times T_{cy(clk)}$	$5.1 + 0.5 \times T_{cy(clk)}$	ns
$t_{h(DYCS)}$	dynamic chip select hold time	$0.3 + 0.5 \times T_{cy(clk)}$	$0.9 + 0.5 \times T_{cy(clk)}$	-	ns
$t_{d(RASV)}$	row address strobe valid delay time	-	$3.1 + 0.5 \times T_{cy(clk)}$	$4.9 + 0.5 \times T_{cy(clk)}$	ns
$t_{h(RAS)}$	row address strobe hold time	$0.5 + 0.5 \times T_{cy(clk)}$	$1.1 + 0.5 \times T_{cy(clk)}$	-	ns
$t_{d(CASV)}$	column address strobe valid delay time	-	$2.9 + 0.5 \times T_{cy(clk)}$	$4.6 + 0.5 \times T_{cy(clk)}$	ns
$t_{h(CAS)}$	column address strobe hold time	$0.3 + 0.5 \times T_{cy(clk)}$	$0.9 + 0.5 \times T_{cy(clk)}$	-	ns
$t_{d(WEV)}$	write enable valid delay time	-	$3.2 + 0.5 \times T_{cy(clk)}$	$5.9 + 0.5 \times T_{cy(clk)}$	ns
$t_{h(WE)}$	write enable hold time	$1.3 + 0.5 \times T_{cy(clk)}$	$1.4 + 0.5 \times T_{cy(clk)}$	-	ns
$t_{d(DQMOUTV)}$	$\overline{\text{DQMOUT}}$ valid delay time	-	$3.1 + 0.5 \times T_{cy(clk)}$	$5.0 + 0.5 \times T_{cy(clk)}$	ns
$t_{h(DQMOUT)}$	$\overline{\text{DQMOUT}}$ hold time	$0.2 + 0.5 \times T_{cy(clk)}$	$0.8 + 0.5 \times T_{cy(clk)}$	-	ns
$t_{d(AV)}$	address valid delay time	-	$3.8 + 0.5 \times T_{cy(clk)}$	$6.3 + 0.5 \times T_{cy(clk)}$	ns
$t_{h(A)}$	address hold time	$0.3 + 0.5 \times T_{cy(clk)}$	$0.9 + 0.5 \times T_{cy(clk)}$	-	ns
$t_{d(CKEOUTV)}$	$\overline{\text{CKEOUT}}$ valid delay time	-	$3.1 + 0.5 \times T_{cy(clk)}$	$5.1 + 0.5 \times T_{cy(clk)}$	ns
$t_{h(CKEOUT)}$	$\overline{\text{CKEOUT}}$ hold time	$0.5 \times T_{cy(clk)}$	$0.7 + 0.5 \times T_{cy(clk)}$	-	ns
Read cycle parameters					
$t_{su(D)}$	data input set-up time	−1.5	−0.5	-	ns
$t_{h(D)}$	data input hold time	-	0.8	2.2	ns
Write cycle parameters					
$t_{d(QV)}$	data output valid delay time	-	$3.8 + 0.5 \times T_{cy(clk)}$	$6.2 + 0.5 \times T_{cy(clk)}$	ns
$t_{h(Q)}$	data output hold time	$0.5 \times T_{cy(clk)}$	$0.7 + 0.5 \times T_{cy(clk)}$	-	ns

Table 23. Dynamic characteristics: Dynamic external memory interface; EMC_CLK[3:0] delay values

T_{amb} = −40 °C to 85 °C; $V_{DD(IO)} = 3.3\ V \pm 10\ \%$; $2.2\ V \leq V_{DD(REG)(3V3)} \leq 3.6\ V$.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_d	delay time	delay value [1]				
		CLKn_DELAY = 0	0.0	0.0	0.0	ns
		CLKn_DELAY = 1 [1]	0.4	0.5	0.8	ns
		CLKn_DELAY = 2 [1]	0.7	1.0	1.7	ns
		CLKn_DELAY = 3 [1]	1.1	1.6	2.5	ns
		CLKn_DELAY = 4 [1]	1.4	2.0	3.3	ns
		CLKn_DELAY = 5 [1]	1.7	2.6	4.1	ns
		CLKn_DELAY = 6 [1]	2.1	3.1	4.9	ns
		CLKn_DELAY = 7 [1]	2.5	3.6	5.8	ns

[1] Program the EMC_CLKn delay values in the EMCDELAYCLK register (see the *LPC18xx User manual*). The delay values must be the same for all SDRAM clocks EMC_CLKn: CLK0_DELAY = CLK1_DELAY = CLK2_DELAY = CLK3_DELAY.



For the programmable EMC_CLK[3:0] clock delays CLKn_DELAY, see Table 23 .

Remark: For SDRAM operation, set CLK0_DELAY = CLK1_DELAY = CLK2_DELAY = CLK3_DELAY in the EMCDELAYCLK register.

Fig 30. SDRAM timing

11.12 USB interface

Table 24. Dynamic characteristics: USB0 and USB1 pins (full-speed)
C_L = 50 pF; R_{pu} = 1.5 kΩ on D+ to $V_{DD(IO)}$, unless otherwise specified; 3.0 V ≤ $V_{DD(IO)}$ ≤ 3.6 V.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_r	rise time	10 % to 90 %		8.5	-	13.8	ns
t_f	fall time	10 % to 90 %		7.7	-	13.7	ns
t_{FRFM}	differential rise and fall time matching	t_r / t_f		-	-	109	%
V_{CRS}	output signal crossover voltage			1.3	-	2.0	V
t_{FEOPT}	source SE0 interval of EOP	see Figure 31		160	-	175	ns
t_{FDEOP}	source jitter for differential transition to SE0 transition	see Figure 31		−2	-	+5	ns
t_{JR1}	receiver jitter to next transition			−18.5	-	+18.5	ns
t_{JR2}	receiver jitter for paired transitions	10 % to 90 %		−9	-	+9	ns
t_{EOPR1}	EOP width at receiver	must reject as EOP; see Figure 31	[1]	40	-	-	ns
t_{EOPR2}	EOP width at receiver	must accept as EOP; see Figure 31	[1]	82	-	-	ns

[1] Characterized but not implemented as production test. Guaranteed by design.

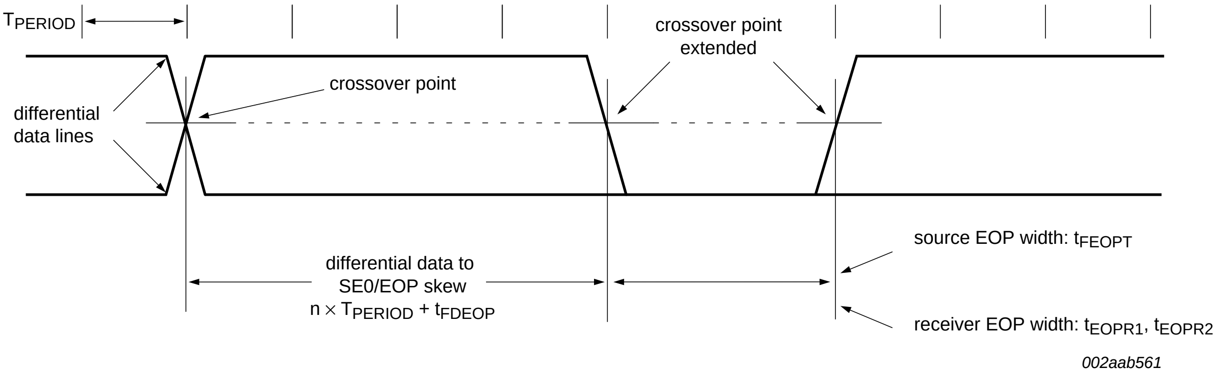


Fig 31. Differential data-to-EOP transition skew and EOP width

Table 25. Static characteristics: USB0 PHY pins[1]

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
High-speed mode							
P_{cons}	power consumption		[2]	-	68	-	mW
$I_{DDA(3V3)}$	analog supply current (3.3 V)	on pin USB0_VDDA3V3_DRIVER;	[3]				
		total supply current		-	18	-	mA
		during transmit		-	31	-	mA
		during receive		-	14	-	mA
		with driver tri-stated		-	14	-	mA
I_{DDD}	digital supply current			-	7	-	mA
Full-speed/low-speed mode							
P_{cons}	power consumption		[2]	-	15	-	mW
$I_{DDA(3V3)}$	analog supply current (3.3 V)	on pin USB0_VDDA3V3_DRIVER;					
		total supply current		-	3.5	-	mA
		during transmit		-	5	-	mA
		during receive		-	3	-	mA
		with driver tri-stated		-	3	-	mA
I_{DDD}	digital supply current			-	3	-	mA
Suspend mode							
$I_{DDA(3V3)}$	analog supply current (3.3 V)			-	24	-	μA
		with driver tri-stated		-	24	-	μA
		with OTG functionality enabled		-	3	-	mA
I_{DDD}	digital supply current			-	30	-	μA
VBUS detector outputs							
V_{th}	threshold voltage	for VBUS valid		4.4	-	-	V
		for session end		0.2	-	0.8	V
		for A valid		0.8	-	2	V
		for B valid		2	-	4	V
V_{hys}	hysteresis voltage	for session end		-	150	10	mV
		A valid		-	200	10	mV
		B valid		-	200	10	mV

[1] Characterized but not implemented as production test.

[2] Total average power consumption.

[3] The driver is active only 20 % of the time.

11.13 Ethernet

Table 26. Dynamic characteristics: Ethernet

T_{amb} = −40 °C to 85 °C, 2.2 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V; 2.7 V ≤ $V_{DD(IO)}$ ≤ 3.6 V. Values guaranteed by design.

Symbol	Parameter	Conditions		Min	Max	Unit
RMII mode						
f_{clk}	clock frequency	for ENET_RX_CLK	[1]	-	50	MHz
δ_{clk}	clock duty cycle		[1]	50	50	%
t_{su}	set-up time	for ENET_TXDn, ENET_TX_EN, ENET_RXDn, ENET_RX_ER, ENET_RX_DV	[1][2]	4	-	ns
t_h	hold time	for ENET_TXDn, ENET_TX_EN, ENET_RXDn, ENET_RX_ER, ENET_RX_DV	[1][2]	2	-	ns
MII mode						
f_{clk}	clock frequency	for ENET_TX_CLK	[1]	-	25	MHz
δ_{clk}	clock duty cycle		[1]	50	50	%
t_{su}	set-up time	for ENET_TXDn, ENET_TX_EN, ENET_TX_ER	[1][2]	4	-	ns
t_h	hold time	for ENET_TXDn, ENET_TX_EN, ENET_TX_ER	[1][2]	2	-	ns
f_{clk}	clock frequency	for ENET_RX_CLK	[1]	-	25	MHz
δ_{clk}	clock duty cycle		[1]	50	50	%
t_{su}	set-up time	for ENET_RXDn, ENET_RX_ER, ENET_RX_DV	[1][2]	4	-	ns
t_h	hold time	for ENET_RXDn, ENET_RX_ER, ENET_RX_DV	[1][2]	2	-	ns

[1] Output drivers can drive a load ≥ 25 pF accommodating over 12 inch of PCB trace and the input capacitance of the receiving device.

[2] Timing values are given from the point at which the clock signal waveform crosses 1.4 V to the valid input or output level.

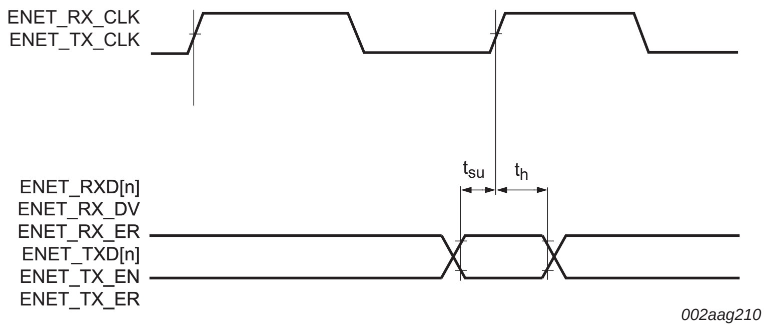


Fig 32. Ethernet timing

11.14 SD/MMC

Table 27. Dynamic characteristics: SD/MMC

T_{amb} = 25 °C, 2.2 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V; 2.7 V ≤ $V_{DD(IO)}$ ≤ 3.6 V, C_L = 20 pF. Simulated values.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{clk}	clock frequency	on pin SD_CLK; data transfer mode	-	40	<tbd>	MHz
		on pin SD_CLK; identification mode			<tbd>	MHz
$t_{su(D)}$	data input set-up time	on pins SD_CMD, SD_DATn as inputs	<tbd>	9.9	-	ns
$t_{h(D)}$	data input hold time	on pins SD_CMD, SD_DATn as inputs	<tbd>	0.3	-	ns
$t_{d(QV)}$	data output valid delay time	on pins SD_CMD, SD_DATn as outputs	-	6.9	<tbd>	ns
$t_{h(Q)}$	data output hold time	on pins SD_CMD, SD_DATn as outputs	<tbd>	0.3	-	ns

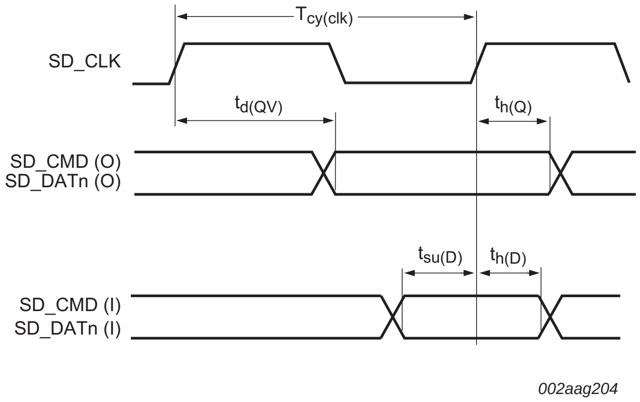


Fig 33. SD/MMC timing

11.15 LCD

Table 28. Dynamic characteristics: LCD

T_{amb} = 25 °C; 2.2 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V; 2.7 V ≤ $V_{DD(IO)}$ ≤ 3.6 V; C_L = 20 pF. Simulated values.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{clk}	clock frequency	on pin LCD_DCLK	-	50	<tbd>	MHz
$t_{su(D)}$	data input set-up time		<tbd>		-	ns
$t_{h(D)}$	data input hold time		<tbd>	<tbd>	-	ns
$t_{d(QV)}$	data output valid delay time		-	14.1	<tbd>	ns
$t_{h(Q)}$	data output hold time		<tbd>	<tbd>	-	ns

12. ADC/DAC electrical characteristics

Table 29. ADC characteristics

$V_{DDA(3V3)}$ over specified ranges; T_{amb} = –40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IA}	analog input voltage			0	-	$V_{DDA(3V3)}$	V
C_{ia}	analog input capacitance			-	-	2	pF
E_D	differential linearity error	$2.7\ V \leq V_{DDA(3V3)} \leq 3.6\ V$	[1][2]	-	±0.8	-	LSB
		$2.2\ V \leq V_{DDA(3V3)} < 2.7\ V$		-	±1.0	-	LSB
$E_{L(adj)}$	integral non-linearity	$2.7\ V \leq V_{DDA(3V3)} \leq 3.6\ V$	[3]	-	±0.8	-	LSB
		$2.2\ V \leq V_{DDA(3V3)} < 2.7\ V$		-	±1.5	-	LSB
E_O	offset error	$2.7\ V \leq V_{DDA(3V3)} \leq 3.6\ V$	[4]	-	±0.15	-	LSB
		$2.2\ V \leq V_{DDA(3V3)} < 2.7\ V$		-	±0.15	-	LSB
E_G	gain error	$2.7\ V \leq V_{DDA(3V3)} \leq 3.6\ V$	[5]	-	±0.3	-	%
		$2.2\ V \leq V_{DDA(3V3)} < 2.7\ V$		-	±0.35	-	%
E_T	absolute error	$2.7\ V \leq V_{DDA(3V3)} \leq 3.6\ V$	[6]	-	±3	-	LSB
		$2.2\ V \leq V_{DDA(3V3)} < 2.7\ V$		-	±4	-	LSB
R_{vsi}	voltage source interface resistance	see Figure 35		-	-	$1/(7 \times f_{clk(ADC)} \times C_{ia})$	kΩ
R_i	input resistance		[7][8]	-	-	1.2	MΩ
$f_{clk(ADC)}$	ADC clock frequency			-	-	4.5	MHz
f_s	sampling frequency	10-bit resolution; 11 clock cycles		-	-	400	kSamples/s
		2-bit resolution; 3 clock cycles				1.5	MSamples/s

[1] The ADC is monotonic, there are no missing codes.

[2] The differential linearity error (E_D) is the difference between the actual step width and the ideal step width. See Figure 34.

[3] The integral non-linearity ($E_{L(adj)}$) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset errors. See Figure 34.

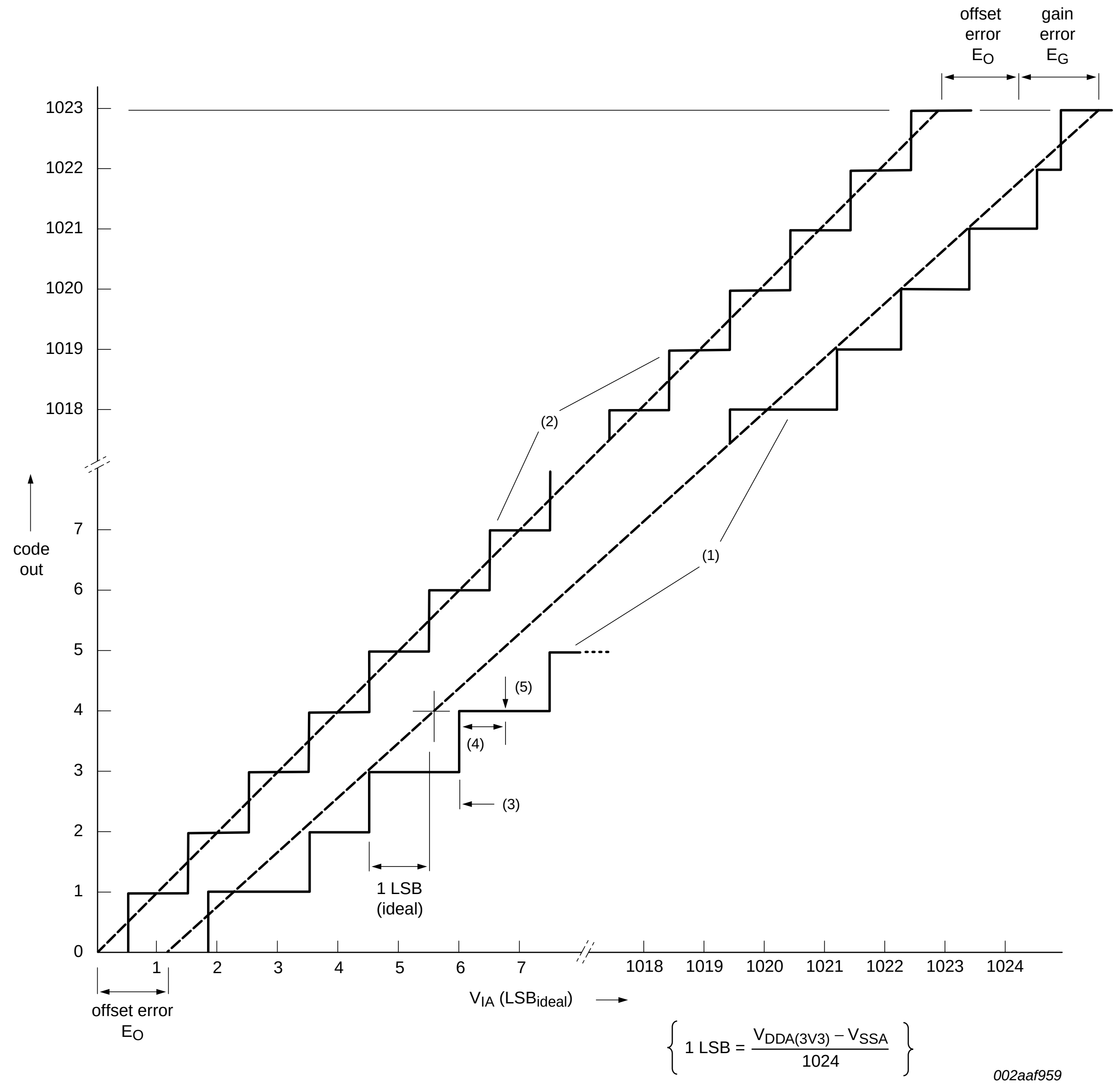
[4] The offset error (E_O) is the absolute difference between the straight line which fits the actual curve and the straight line which fits the ideal curve. See Figure 34.

[5] The gain error (E_G) is the relative difference in percent between the straight line fitting the actual transfer curve after removing offset error, and the straight line which fits the ideal transfer curve. See Figure 34.

[6] The absolute error (E_T) is the maximum difference between the center of the steps of the actual transfer curve of the non-calibrated ADC and the ideal transfer curve. See Figure 34.

[7] T_{amb} = 25 °C.

[8] Input resistance R_i depends on the sampling frequency fs: $R_i = 2\ k\Omega + 1 / (f_s \times C_{ia})$.



(1) Example of an actual transfer curve.

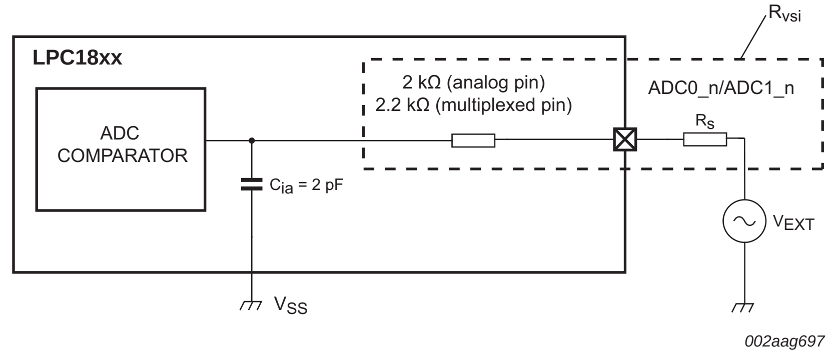
(2) The ideal transfer curve.

(3) Differential linearity error (E_D).

(4) Integral non-linearity ($E_{L(adj)}$).

(5) Center of a step of the actual transfer curve.

Fig 34. 10-bit ADC characteristics



$R_s < 1/((7 \times f_{clk(ADC)} \times C_{ia}) - 2\ k\Omega$

Fig 35. ADC interface to pins

Table 30. DAC characteristics

$V_{DDA(3V3)}$ *over specified ranges;* T_{amb} *= −40 °C to +85 °C; unless otherwise specified*

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
E_D	differential linearity error	$2.7\ V \le V_{DDA(3V3)} \le 3.6\ V$	[1]	-	±0.8	-	LSB
		$2.2\ V \le V_{DDA(3V3)} < 2.7\ V$		-	±1.0	-	LSB
$E_{L(adj)}$	integral non-linearity	code = 0 to 975 $2.7\ V \le V_{DDA(3V3)} \le 3.6\ V$	[1]	-	±1.0	-	LSB
		$2.2\ V \le V_{DDA(3V3)} < 2.7\ V$		-	±1.5	-	LSB
E_O	offset error	$2.7\ V \le V_{DDA(3V3)} \le 3.6\ V$	[1]	-	±0.8	-	LSB
		$2.2\ V \le V_{DDA(3V3)} < 2.7\ V$		-	±1.0	-	LSB
E_G	gain error	$2.7\ V \le V_{DDA(3V3)} \le 3.6\ V$	[1]	-	±0.3	-	%
		$2.2\ V \le V_{DDA(3V3)} < 2.7\ V$		-	±1.0	-	%
C_L	load capacitance			-	-	200	pF
R_L	load resistance			1	-	-	kΩ
t_s	settling time		[1]		0.4		µs

[1] In the DAC CR register, bit BIAS = 0 (see the *LPC18xx user manual*).

[2] Settling time is calculated within 1/2 LSB of the final value.

13. Application information

13.1 LCD panel signal usage

Table 31. LCD panel connections for STN single panel mode

External pin	4-bit mono STN single panel		8-bit mono STN single panel		Color STN single panel	
	LPC18xx pin used	LCD function	LPC18xx pin used	LCD function	LPC18xx pin used	LCD function
LCD_VD[23:8]	-	-	-	-	-	-
LCD_VD7	-	-	P8_4	UD[7]	P8_4	UD[7]
LCD_VD6	-	-	P8_5	UD[6]	P8_5	UD[6]
LCD_VD5	-	-	P8_6	UD[5]	P8_6	UD[5]
LCD_VD4	-	-	P8_7	UD[4]	P8_7	UD[4]
LCD_VD3	P4_2	UD[3]	P4_2	UD[3]	P4_2	UD[3]
LCD_VD2	P4_3	UD[2]	P4_3	UD[2]	P4_3	UD[2]
LCD_VD1	P4_4	UD[1]	P4_4	UD[1]	P4_4	UD[1]
LCD_VD0	P4_1	UD[0]	P4_1	UD[0]	P4_1	UD[0]
LCD_LP	P7_6	LCDLP	P7_6	LCDLP	P7_6	LCDLP
LCD_ENAB/ LCDM	P4_6	LCDENAB/ LCDM	P4_6	LCDENAB/ LCDM	P4_6	LCDENAB/ LCDM
LCD_FP	P4_5	LCDFP	P4_5	LCDFP	P4_5	LCDFP
LCD_DCLK	P4_7	LCDDCLK	P4_7	LCDDCLK	P4_7	LCDDCLK
LCD_LE	P7_0	LCDLE	P7_0	LCDLE	P7_0	LCDLE
LCD_PWR	P7_7	CDPWR	P7_7	LCDPWR	P7_7	LCDPWR
GP_CLKIN	PF_4	LCDCLKIN	PF_4	LCDCLKIN	PF_4	LCDCLKIN

Table 32. LCD panel connections for STN dual panel mode

External pin	4-bit mono STN dual panel		8-bit mono STN dual panel		Color STN dual panel	
	LPC18xx pin used	LCD function	LPC18xx pin used	LCD function	LPC18xx pin used	LCD function
LCD_VD[23:16]	-	-	-	-	-	-
LCD_VD15	-	-	PB_4	LD[7]	PB_4	LD[7]
LCD_VD14	-	-	PB_5	LD[6]	PB_5	LD[6]
LCD_VD13	-	-	PB_6	LD[5]	PB_6	LD[5]
LCD_VD12	-	-	P8_3	LD[4]	P8_3	LD[4]
LCD_VD11	P4_9	LD[3]	P4_9	LD[3]	P4_9	LD[3]
LCD_VD10	P4_10	LD[2]	P4_10	LD[2]	P4_10	LD[2]
LCD_VD9	P4_8	LD[1]	P4_8	LD[1]	P4_8	LD[1]
LCD_VD8	P7_5	LD[0]	P7_5	LD[0]	P7_5	LD[0]
LCD_VD7	-	-		UD[7]	P8_4	UD[7]
LCD_VD6	-	-	P8_5	UD[6]	P8_5	UD[6]
LCD_VD5	-	-	P8_6	UD[5]	P8_6	UD[5]
LCD_VD4	-	-	P8_7	UD[4]	P8_7	UD[4]
LCD_VD3	P4_2	UD[3]	P4_2	UD[3]	P4_2	UD[3]

Table 32. LCD panel connections for STN dual panel mode

External pin	4-bit mono STN dual panel		8-bit mono STN dual panel		Color STN dual panel	
	LPC18xx pin used	LCD function	LPC18xx pin used	LCD function	LPC18xx pin used	LCD function
LCD_VD2	P4_3	UD[2]	P4_3	UD[2]	P4_3	UD[2]
LCD_VD1	P4_4	UD[1]	P4_4	UD[1]	P4_4	UD[1]
LCD_VD0	P4_1	UD[0]	P4_1	UD[0]	P4_1	UD[0]
LCD_LP	P7_6	LCDLP	P7_6	LCDLP	P7_6	LCDLP
LCD_ENAB/ LCDM	P4_6	LCDENAB/ LCDM	P4_6	LCDENAB/ LCDM	P4_6	LCDENAB/ LCDM
LCD_FP	P4_5	LCDFP	P4_5	LCDFP	P4_5	LCDFP
LCD_DCLK	P4_7	LCDDCLK	P4_7	LCDDCLK	P4_7	LCDDCLK
LCD_LE	P7_0	LCDLE	P7_0	LCDLE	P7_0	LCDLE
LCD_PWR	P7_7	LCDPWR	P7_7	LCDPWR	P7_7	LCDPWR
GP_CLKIN	PF_4	LCDCLKIN	PF_4	LCDCLKIN	PF_4	LCDCLKIN

Table 33. LCD panel connections for TFT panels

External pin	TFT 12 bit (4:4:4 mode)		TFT 16 bit (5:6:5 mode)		TFT 16 bit (1:5:5:5 mode)		TFT 24 bit	
	LPC18xx pin used	LCD function	LPC18xx pin used	LCD function	LPC18xx pin used	LCD function	LPC18xx pin used	LCD function
LCD_VD23	PB_0	BLUE3	PB_0	BLUE4	PB_0	BLUE4		BLUE7
LCD_VD22	PB_1	BLUE2	PB_1	BLUE3	PB_1	BLUE3		BLUE6
LCD_VD21	PB_2	BLUE1	PB_2	BLUE2	PB_2	BLUE2		BLUE5
LCD_VD20	PB_3	BLUE0	PB_3	BLUE1	PB_3	BLUE1		BLUE4
LCD_VD19	-	-	P7_1	BLUE0	P7_1	BLUE0		BLUE3
LCD_VD18	-	-	-	-	P7_2	intensity		BLUE2
LCD_VD17	-	-	-	-	-	-	P7_3	BLUE1
LCD_VD16	-	-	-	-	-	-	P7_4	BLUE0
LCD_VD15	PB_4	GREEN3	PB_4	GREEN5	PB_4	GREEN4	PB_4	GREEN7
LCD_VD14	PB_5	GREEN2	PB_5	GREEN4	PB_5	GREEN3	PB_5	GREEN6
LCD_VD13	PB_6	GREEN1	PB_6	GREEN3	PB_6	GREEN2	PB_6	GREEN5
LCD_VD12	P8_3	GREEN0	P8_3	GREEN2	P8_3	GREEN1	P8_3	GREEN4
LCD_VD11	-	-	P4_9	GREEN1	P4_9	GREEN0	P4_9	GREEN3
LCD_VD10	-	-	P4_10	GREEN0	P4_10	intensity	P4_10	GREEN2
LCD_VD9	-	-	-	-	-	-	P4_8	GREEN1
LCD_VD8	-	-	-	-	-	-	P7_5	GREEN0
LCD_VD7	P8_4	RED3	P8_4	RED4	P8_4	RED4	P8_4	RED7
LCD_VD6	P8_5	RED2	P8_5	RED3	P8_5	RED3	P8_5	RED6
LCD_VD5	P8_6	RED1	P8_6	RED2	P8_6	RED2	P8_6	RED5
LCD_VD4	P8_7	RED0	P8_7	RED1	P8_7	RED1	P8_7	RED4
LCD_VD3	-	-	P4_2	RED0	P4_2	RED0	P4_2	RED3
LCD_VD2	-	-	-	-	P4_3	intensity	P4_3	RED2
LCD_VD1	-	-	-	-	-	-	P4_4	RED1

Table 33. LCD panel connections for TFT panels

External pin	TFT 12 bit (4:4:4 mode)		TFT 16 bit (5:6:5 mode)		TFT 16 bit (1:5:5:5 mode)		TFT 24 bit	
	LPC18xx pin used	LCD function	LPC18xx pin used	LCD function	LPC18xx pin used	LCD function	LPC18xx pin used	LCD function
LCD_VD0	-	-	-	-	-	-	P4_1	RED0
LCD_LP	P7_6	LCDLP	P7_6	LCDLP	P7_6	LCDLP	P7_6	LCDLP
LCD_ENAB /LCDM	P4_6	LCDENAB/ LCDM	P4_6	LCDENAB/ LCDM	P4_6	LCDENAB/ LCDM	P4_6	LCDENAB/ LCDM
LCD_FP	P4_5	LCDFP	P4_5	LCDFP	P4_5	LCDFP	P4_5	LCDFP
LCD_DCLK	P4_7	LCDDCLK	P4_7	LCDDCLK	P4_7	LCDDCLK	P4_7	LCDDCLK
LCD_LE	P7_0	LCDLE	P7_0	LCDLE	P7_0	LCDLE	P7_0	LCDLE
LCD_PWR	P7_7	LCDPWR	P7_7	LCDPWR	P7_7	LCDPWR	P7_7	LCDPWR
GP_CLKIN	PF_4	LCDCLKIN	PF_4	LCDCLKIN	PF_4	LCDCLKIN	PF_4	LCDCLKIN

13.2 Crystal oscillator

The crystal oscillator is controlled by the XTAL_OSC_CTRL register in the CGU (see *LPC18xx user manual*).

The crystal oscillator operates at frequencies of 1 MHz to 25 MHz. This frequency can be boosted to a higher frequency, up to the maximum CPU operating frequency, by the PLL.

The oscillator can operate in one of two modes: slave mode and oscillation mode.

- In slave mode, couple the input clock signal with a capacitor of 100 pF (C_C in Figure 36), with an amplitude of at least 200 mV (RMS). The XTAL2 pin in this configuration can be left unconnected.
- External components and models used in oscillation mode are shown in Figure 37, and in Table 34 and Table 35. Since the feedback resistance is integrated on chip, only a crystal and the capacitances C_{X1} and C_{X2} need to be connected externally in case of fundamental mode oscillation (L, C_L and R_S represent the fundamental frequency). Capacitance C_P in Figure 37 represents the parallel package capacitance and must not be larger than 7 pF. Parameters F_C, C_L, R_S and C_P are supplied by the crystal manufacturer.

Table 34. Recommended values for $C_{X1/X2}$ in oscillation mode (crystal and external components parameters) low frequency mode

Fundamental oscillation frequency	Maximum crystal series resistance R_S	External load capacitors C_{X1}, C_{X2}
2 MHz	< 200 Ω	33 pF, 33 pF
	< 200 Ω	39 pF, 39 pF
	< 200 Ω	56 pF, 56 pF
4 MHz	< 200 Ω	18 pF, 18 pF
	< 200 Ω	39 pF, 39 pF
	< 200 Ω	56 pF, 56 pF
8 MHz	< 200 Ω	18 pF, 18 pF
	< 200 Ω	39 pF, 39 pF

Table 34. Recommended values for $C_{X1/X2}$ in oscillation mode (crystal and external components parameters) low frequency mode

Fundamental oscillation frequency	Maximum crystal series resistance R_S	External load capacitors C_{X1}, C_{X2}
12 MHz	< 160 Ω	18 pF, 18 pF
	< 160 Ω	39 pF, 39 pF
16 MHz	< 120 Ω	18 pF, 18 pF
	< 80 Ω	33 pF, 33 pF
20 MHz	< 100 Ω	18 pF, 18 pF
	< 80 Ω	33 pF, 33 pF

Table 35. Recommended values for $C_{X1/X2}$ in oscillation mode (crystal and external components parameters) high frequency mode

Fundamental oscillation frequency	Maximum crystal series resistance R_S	External load capacitors C_{X1}, C_{X2}
15 MHz	< 80 Ω	18 pF, 18 pF
20 MHz	< 80 Ω	39 pF, 39 pF
	< 100 Ω	47 pF, 47 pF

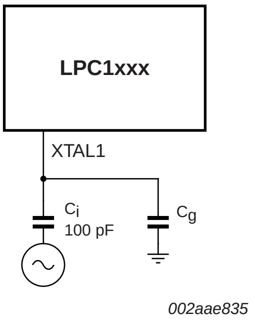


Fig 36. Slave mode operation of the on-chip oscillator

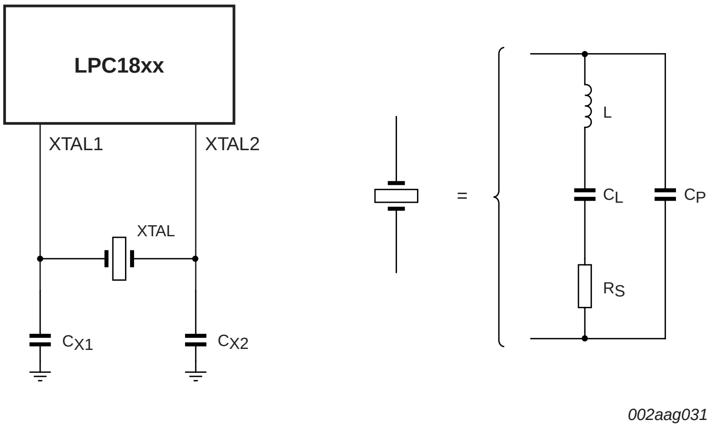


Fig 37. Oscillator modes with external crystal model used for C_{X1}/C_{X2} evaluation

13.3 RTC oscillator

In the RTC oscillator circuit, only the crystal (XTAL) and the capacitances C_{RTCX1} and C_{RTCX2} need to be connected externally. Typical capacitance values for C_{RTCX1} and C_{RTCX2} are $C_{RTCX1/2}$ = 20 (typical) ± 4 pF.

An external clock can be connected to RTCX1 if RTCX2 is left open. The recommended amplitude of the clock signal is $V_{i(RMS)}$ = 100 mV to 200 mV with a coupling capacitance of 5 pF to 10 pF.

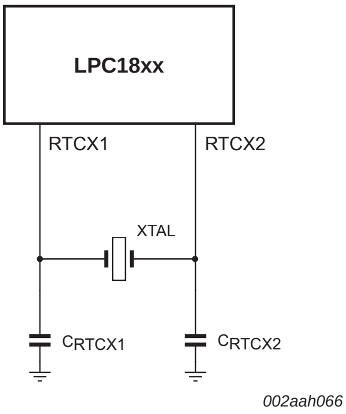


Fig 38. RTC 32 kHz oscillator circuit

13.4 XTAL and RTCX Printed Circuit Board (PCB) layout guidelines

Connect the crystal on the PCB as close as possible to the oscillator input and output pins of the chip. Take care that the load capacitors C_{X1}, C_{X2}, and C_{X3} in case of third overtone crystal usage have a common ground plane. Also connect the external components to the ground plain. To keep the noise coupled in via the PCB as small as possible, make loops and parasitics as small as possible. Choose smaller values of C_{X1} and C_{X2} if parasitics increase in the PCB layout.

Ensure no high-speed or high-drive signals are near the RTCX1/2 signals.

13.5 Standard I/O pin configuration

Figure 39 shows the possible pin modes for standard I/O pins with analog input function:

- Digital output driver enabled/disabled
- Digital input: Pull-up enabled/disabled
- Digital input: Pull-down enabled/disabled
- Digital input: Repeater mode enabled/disabled
- Digital input: Input buffer enabled/disabled
- Analog input

The default configuration for standard I/O pins is input buffer disabled and pull-up enabled. The weak MOS devices provide a drive capability equivalent to pull-up and pull-down resistors.

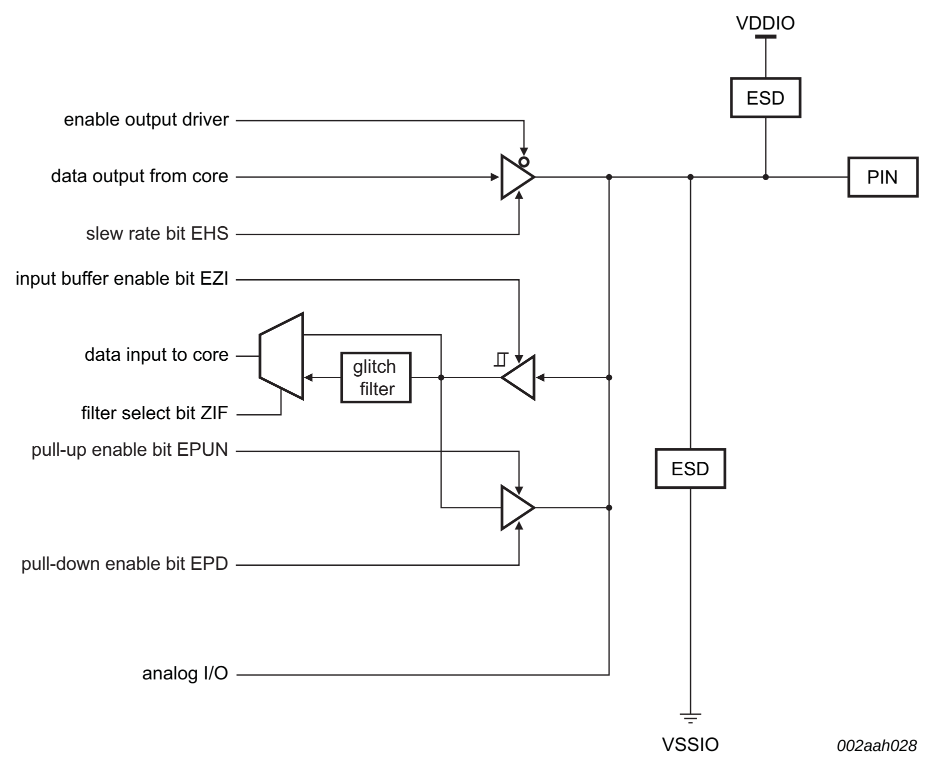


Fig 39. Standard I/O pin configuration with analog input

13.6 Reset pin configuration

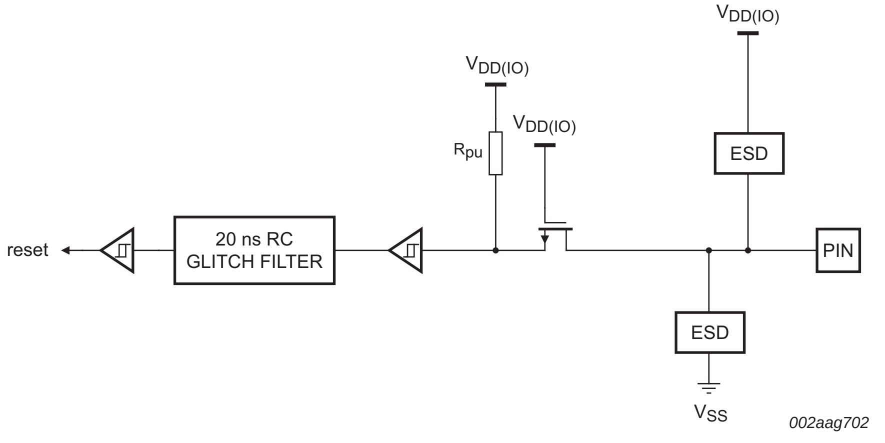
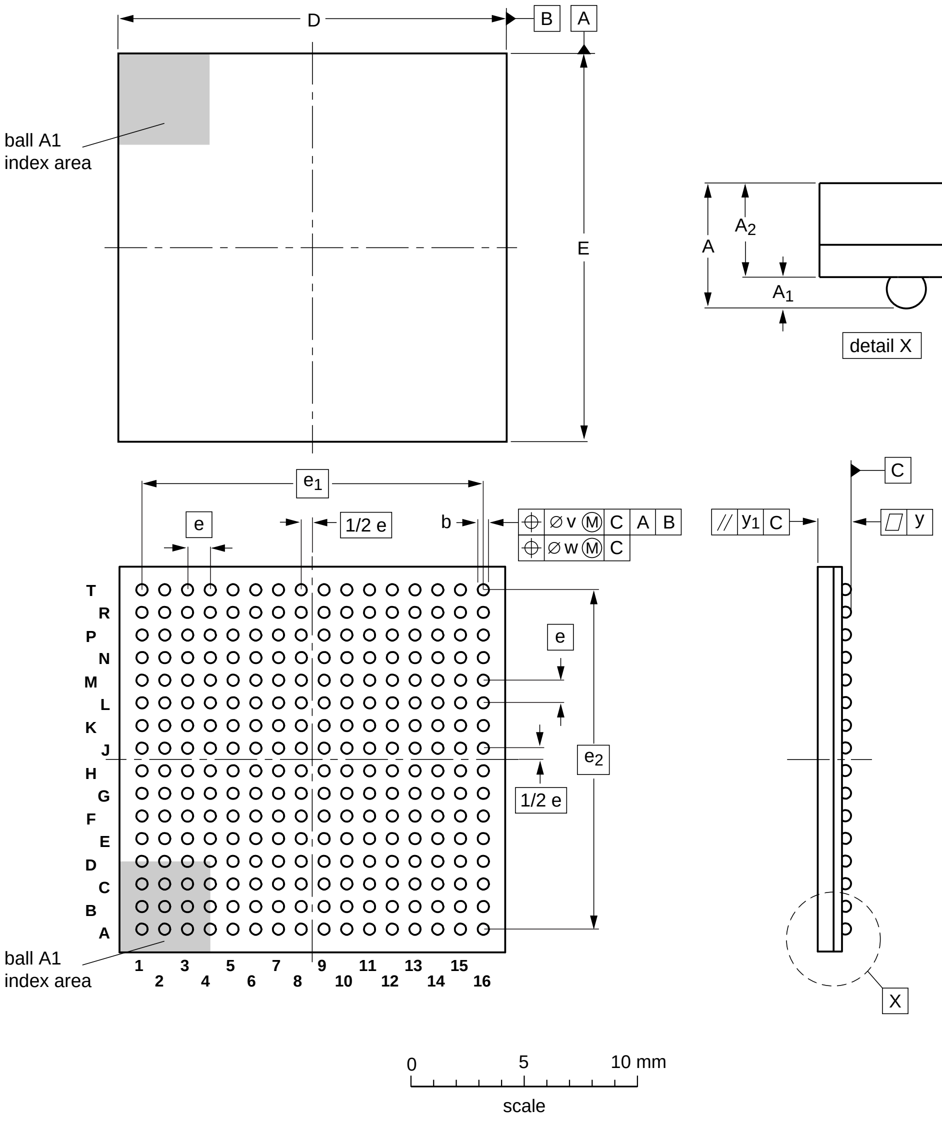


Fig 40. Reset pin configuration

14. Package outline

LBGA256: plastic low profile ball grid array package; 256 balls; body 17 x 17 x 1 mm **SOT740-2**



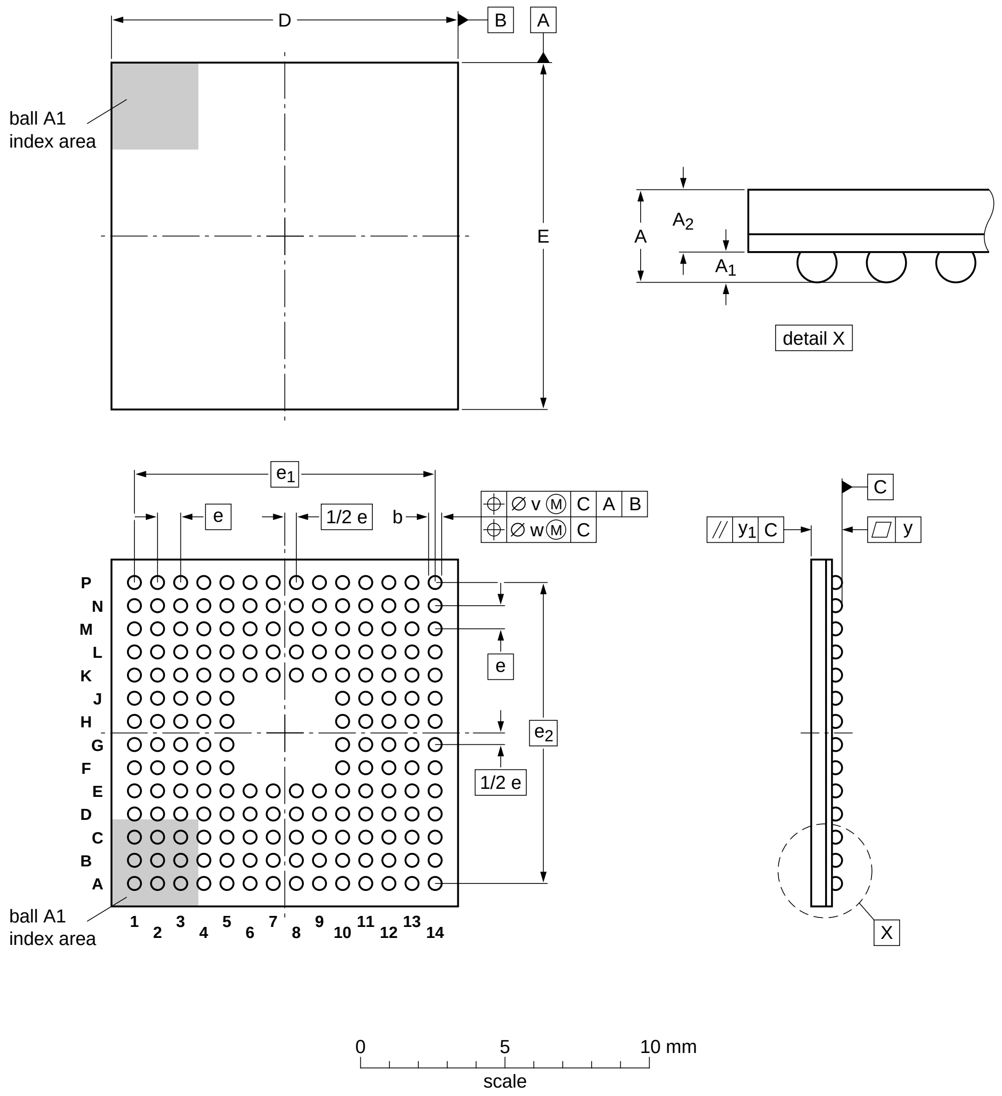
DIMENSIONS (mm are the original dimensions)

UNIT	A max	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
mm	1.55	0.45 0.35	1.1 0.9	0.55 0.45	17.2 16.8	17.2 16.8	1	15	15	0.25	0.1	0.12	0.35

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT740-2	- - -	MO-192	- - -			~~05-06-16~~ 05-08-04

Fig 41. Package outline of the LBGA256 package

TFBGA180: thin fine-pitch ball grid array package; 180 balls **SOT570-3**



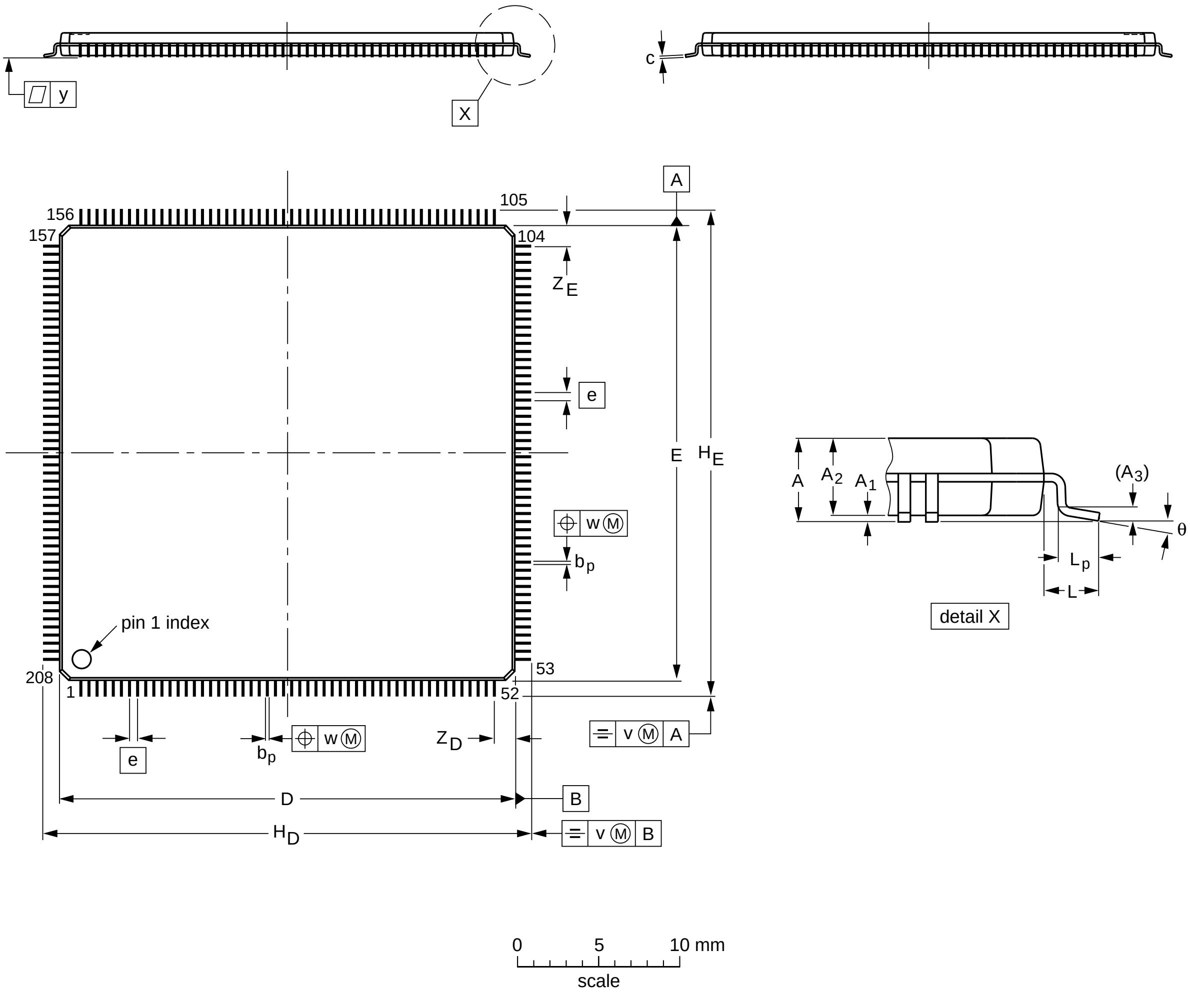
DIMENSIONS (mm are the original dimensions)

UNIT		A	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
mm	max	1.20	0.40	0.80	0.50	12.1	12.1	0.8	10.4	10.4	0.15	0.05	0.12	0.1
	nom	1.06	0.35	0.71	0.45	12.0	12.0							
	min	0.95	0.30	0.65	0.40	11.9	11.9							

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT570-3						~~08-07-09~~ 10-04-15

Fig 42. Package outline of the TFBGA180 package

LQFP208; plastic low profile quad flat package; 208 leads; body 28 x 28 x 1.4 mm **SOT459-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	Z_D	Z_E	θ
mm	1.6	0.15 0.05	1.45 1.35	0.25	0.27 0.17	0.20 0.09	28.1 27.9	28.1 27.9	0.5	30.15 29.85	30.15 29.85	1	0.75 0.45	0.12	0.08	0.08	1.43 1.08	1.43 1.08	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

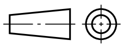
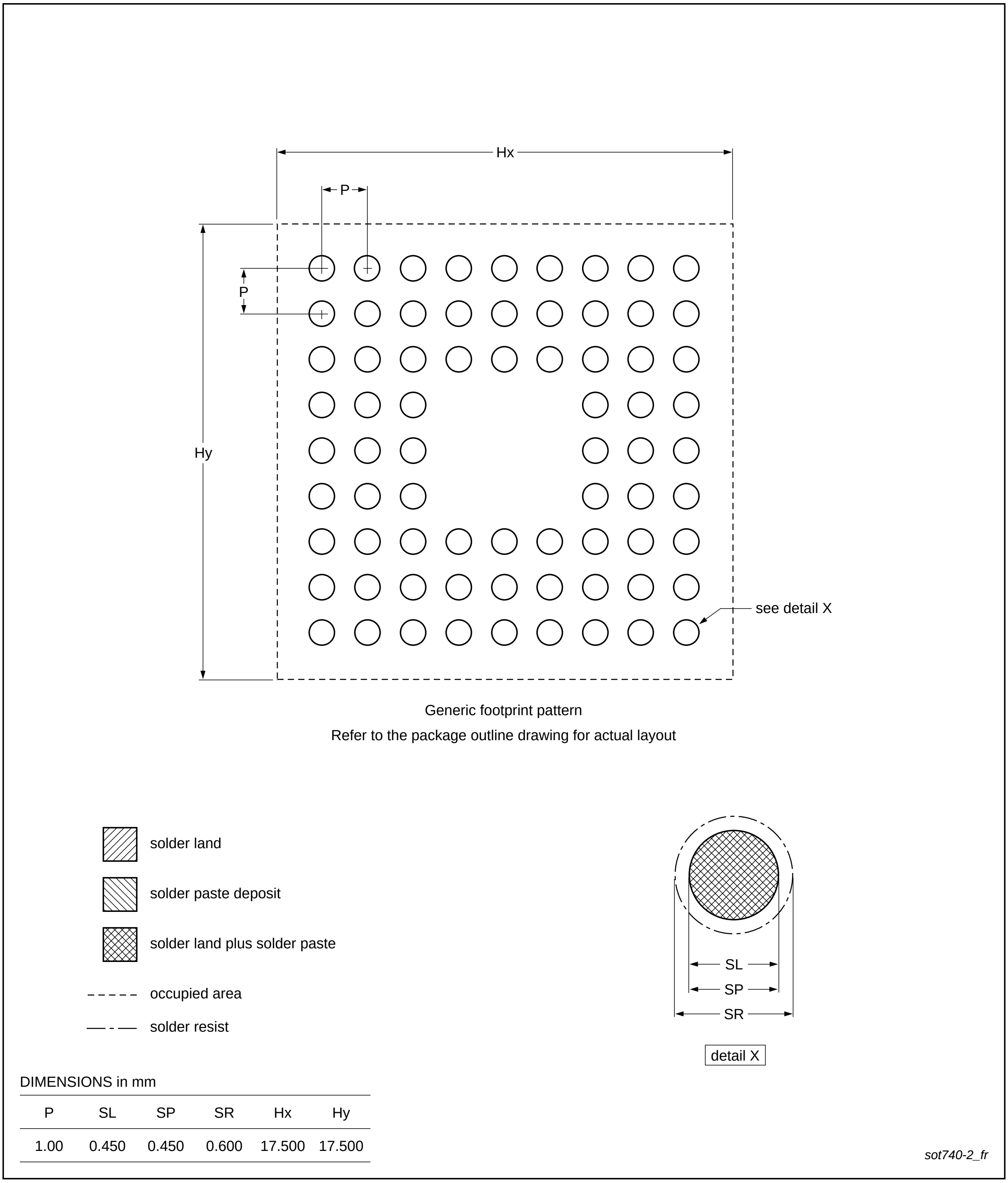
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT459-1	136E30	MS-026				~~00-02-06~~ 03-02-20

Fig 43. Package outline of the LQFP208 package

15. Soldering

Footprint information for reflow soldering of LBGA256 package **SOT740-2**

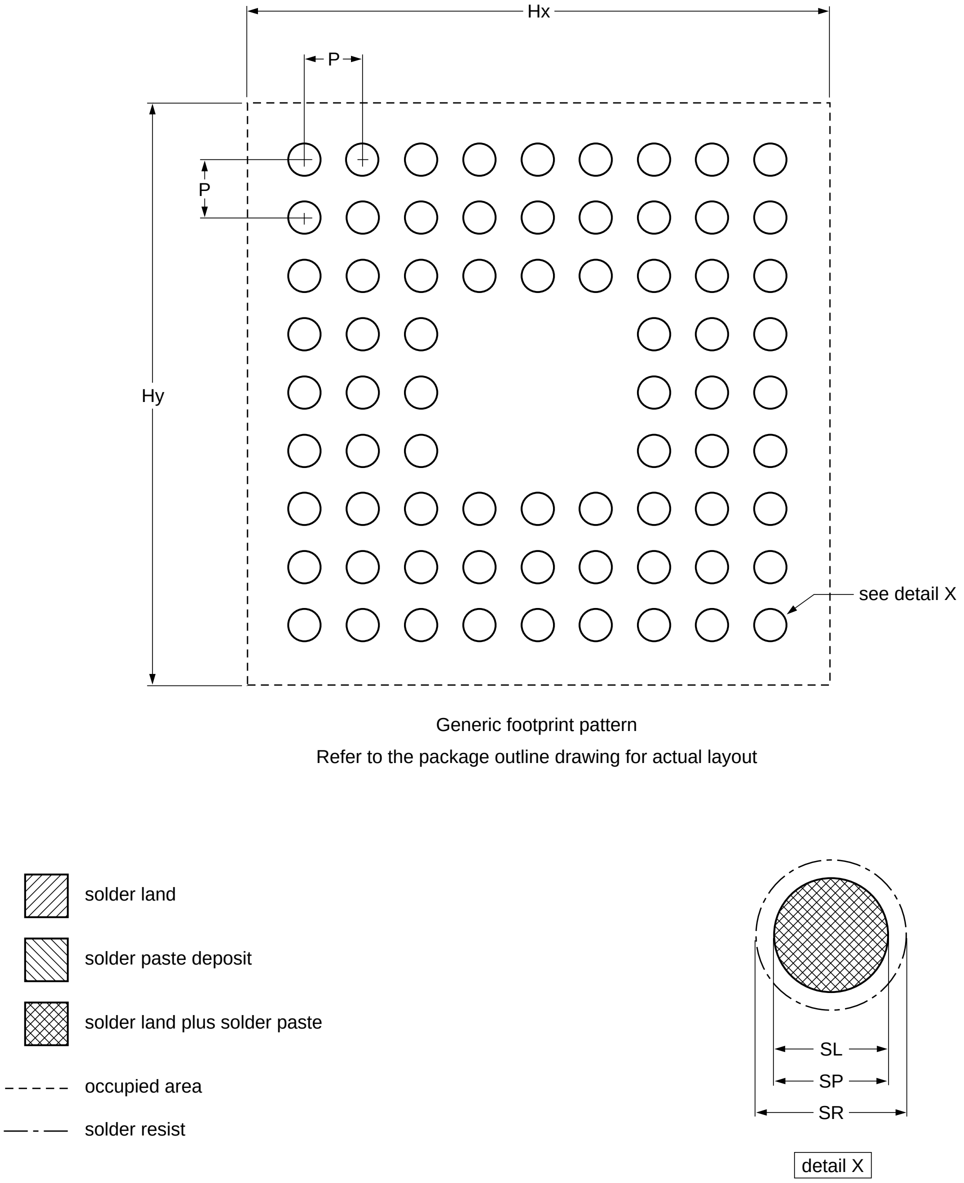


DIMENSIONS in mm

P	SL	SP	SR	Hx	Hy
1.00	0.450	0.450	0.600	17.500	17.500

Fig 44. Reflow soldering for the LBGA256 package

Footprint information for reflow soldering of TFBGA180 package **SOT570-3**



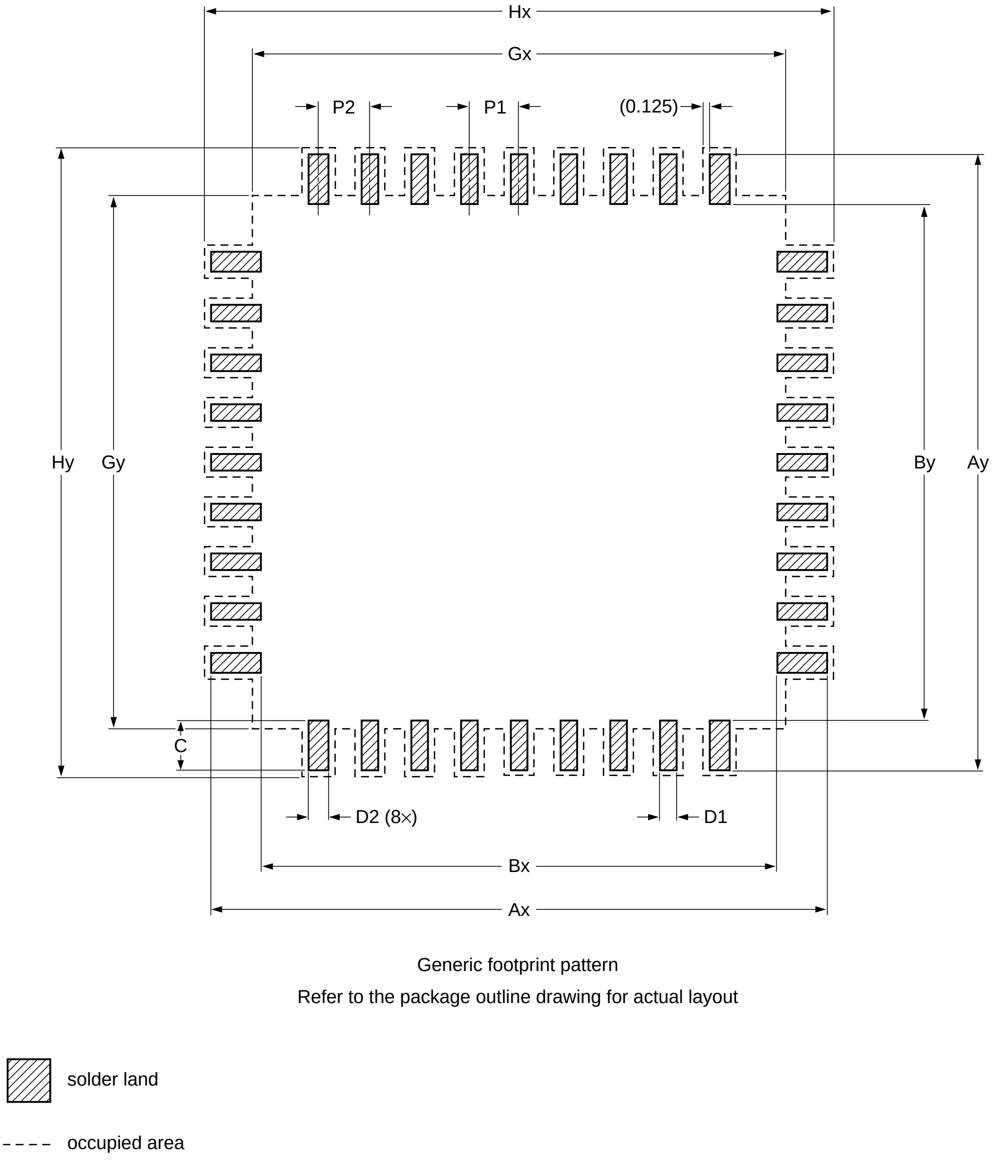
DIMENSIONS in mm

P	SL	SP	SR	Hx	Hy
0.80	0.400	0.400	0.550	12.575	12.575

sot570-3_fr

Fig 45. Reflow soldering for the TFBGA180 package

Footprint information for reflow soldering of LQFP208 package **SOT459-1**



Generic footprint pattern

Refer to the package outline drawing for actual layout

DIMENSIONS in mm

P1	P2	Ax	Ay	Bx	By	C	D1	D2	Gx	Gy	Hx	Hy
0.500	0.560	31.300	31.300	28.300	28.300	1.500	0.280	0.400	28.500	28.500	31.550	31.550

sot459-1_fr

Fig 46. Reflow soldering for the LQFP208 package

16. Abbreviations

Table 36. Abbreviations

Acronym	Description
ADC	Analog-to-Digital Converter
AES	Advanced Encryption Standard
AHB	Advanced High-performance Bus
APB	Advanced Peripheral Bus
API	Application Programming Interface
BOD	BrownOut Detection
BGA	Ball Grid Array
CAN	Controller Area Network
CMAC	Cipher-based Message Authentication Code
CSMA/CD	Carrier Sense Multiple Access with Collision Detection
DAC	Digital-to-Analog Converter
DMA	Direct Memory Access
EOP	End Of Packet
ETB	Embedded Trace Buffer
ETM	Embedded Trace Macrocell
GPIO	General Purpose Input/Output
IRC	Internal RC
IrDA	Infrared Data Association
JTAG	Joint Test Action Group
LCD	Liquid Crystal Display
LSB	Least Significant Bit
LQFP	Low Quad Flat Package
MAC	Media Access Control
MCU	MicroController Unit
MIIM	Media Independent Interface Management
n.c.	not connected
OTG	On-The-Go
PHY	PHYsical layer
PLL	Phase-Locked Loop
PWM	Pulse Width Modulator
RMII	Reduced Media Independent Interface
SDRAM	Synchronous Dynamic Random Access Memory
SPI	Serial Peripheral Interface
SSI	Serial Synchronous Interface
SSP	Synchronous Serial Port
TCP/IP	Transmission Control Protocol/Internet Protocol
TTL	Transistor-Transistor Logic
UART	Universal Asynchronous Receiver/Transmitter
ULPI	UTMI+ Low Pin Interface

Table 36. Abbreviations *…continued*

Acronym	Description
USART	Universal Synchronous Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
UTMI	USB 2.0 Transceiver Macrocell Interface

17. Revision history

Table 37. Revision history

<table>
<tr><th>Document ID</th><th>Release date</th><th>Data sheet status</th><th>Change notice</th><th>Supersedes</th></tr>
<tr><td>LPC1857_53 v.2</td><td>20120515</td><td>Objective data sheet</td><td>-</td><td>LPC1857_53 v.1</td></tr>
<tr><td>Modifications:</td><td colspan="4">• Condition $V_{DD(IO)}$ = 5 V added to parameter I_{IH} in Table 8.
• EEPROM memory location corrected in Figure 6.
• EEPROM user accessible area defined in Section 7.10.
• Condition for INL updated in Table 30.
• Type of USB0_PWR_FAULT and USB1_PWR_FAULT functions changed to I (input) in Table 3.
• BOD trip levels added in Table 9.
• Flash/EEPROM characteristics added (see Section 11.1).
• Pin description for multiplexed analog functions updated in Table 3.
• GPIO configurable open-drain mode removed.
• Table 8 updated (multiple parameters).
• Table 20 updated (multiple parameters).
• Table 21 to Table 23 updated (multiple parameters).
• Table 26 updated (multiple parameters).
• Table 28 added.
• Table 19 added.
• EEPROM timing and characterization added (see Table 11).
• Flash characteristics updated (Table 10).
• $V_{DD(REG)(3V3)}$ limits added for flash read and erase/program operations (see Table 8).
• TFBGA180 pinout added in Table 3.
• Ethernet TCP/IP hardware checksum feature removed.
• Recommendations for connecting an external clock to the RTC oscillator added (see Section 13.3).
• Minimum pulse length for signal on WAKEUPn pins specified in Table 3.
• SPIFI driver removed from boot ROM.
• SPIFI data rate changed to 60 MB/s.
• V_I corrected for USB1_DP and USB1_DM in Table 6.
• Maximum input voltage for 5 V tolerant pins specified as 3.6 V when VDDIO not present.
• USB SOF frame length adjust feature added.
• SCT/timer ORed outputs updated in Table 3 for CTOUT_1, CTOUT_4, CTOUT_5, CTOUT_9, CTOUT_10, CTOUT_12, and CTOUT_13.</td></tr>
<tr><td>LPC1857_53 v.1</td><td>20111214</td><td>Objective data sheet</td><td>-</td><td>-</td></tr>
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18. Legal information

18.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term ‘short data sheet’ is explained in section “Definitions”.

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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